2014-1578

In The United States Court Of Appeals For The Federal Circuit

VICOR CORPORATION,

Appellant,

v.

SYNQOR, INC.,

Appellee.

Appeal from the Patent and Trademark Office – Patent Trial and Appeal Board in Reexamination No. 95/001,702

BRIEF OF APPELLANT

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CERTIFICATE OF INTEREST

Pursuant to Federal Rule of Appellate Procedure 26.1 and Federal Circuit Rule 47.4, the undersigned counsel for Requester-Appellant Vicor Corporation hereby certifies that:

1. The full names of every party or amicus represented by me is:

   VICOR CORPORATION.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

   None.

3. The parent companies, subsidiaries (except wholly-owned subsidiaries), and affiliates that have issued shares to the public, of the party or amicus represented by me are:

   None.

4. The names of all law firms and the partners and associates that appeared for any of the parties represented by me in the District Court or are expected to appear in this Court are:

   Matthew A. Smith of Turner Boyd LLP, 702 Marshall Street, Suite 640, Redwood City, CA 94063.

   Mr. Smith was with Foley & Lardner LLP in Washington, D.C. during some of the proceedings below. Appearing below was also Christopher (Max) Colice, then with Foley & Lardner LLP.

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STATEMENT OF RELATED CASES

No appeal in or from this proceeding was previously before this or any other appellate court.

This Court has rendered one decision in an appeal from a jury trial concerning the same patent. *See SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365 (Fed. Cir. 2013). The Appellant was not a party to that case.

JURISDICTIONAL STATEMENT

The United States Patent & Trademark Office Patent Trial and Appeal Board ("the PTAB") had jurisdiction under 35 U.S.C. § 134. The PTAB mailed its decision on April 10, 2014 (A1-A26). Requester Vicor Corporation ("Vicor") filed a Notice of Appeal on May 20, 2014 in accordance with 28 U.S.C. § 2107 and Fed. R. App. P. 4. The appeal was docketed on July 1, 2014. The Notice of Appeal was timely filed pursuant to 35 U.S.C. § 142. This Court has jurisdiction under 35 U.S.C. § 141 and 28 U.S.C. § 1295(a)(4)(A).

STATEMENT OF THE ISSUES

I. Did the PTAB err by reversing the Examiner's finding that Steigerwald '090 (incorporating Steigerwald '539 by reference) anticipates claims 20-23, 27, 29, 30, 32 and 33 of the '190 patent?

II. Did the PTAB err by reversing the Examiner's finding that claims 24-26 of the '190 patent were obvious over Steigerwald '090 (incorporating Steigerwald '539 by reference)?

III. Did the PTAB err by reversing the Examiner's finding that claims 1-19, 24, 28 and 31 were obvious over Steigerwald '090 (incorporating Steigerwald '539 by reference) in view of Cobos and/or Pressman?

IV. Did the PTAB err by reversing the Examiner's finding that claims 1-38 were obvious over Cobos in view of Pressman?

STATEMENT OF THE CASE

This is an appeal from a decision of the PTAB in an *inter partes* reexamination of U.S. Pat. 7,072,190 ("the '190 patent"). The '190 patent is purportedly owned by SynQor, Inc. of Boxborough, Massachusetts (hereinafter "SynQor"). Vicor Corporation, the third party requester, is headquartered about thirty miles away in Andover, Massachusetts. Vicor and SynQor are competitors in some markets for products related to electrical power supplies. SynQor has also sued Vicor for infringement of the '190 patent in the United States District Court for the Eastern District of Texas.

A. BACKGROUND AND STATEMENT OF FACTS

1). Introduction to the Technology

This case is about DC-DC power converters. (A37, '190 patent, col. 4, ll. 4-12). A DC-DC power converter is a device— somewhat smaller than a modern smartphone—that can be wired onto a circuit board. (A3416, left column). The circuit board will typically have other components, such as computer chips. (*Id.*) These other components require electrical power to operate, often at different voltage levels. (*Id.*). For example, a given circuit board might have two chips, one requiring a 1-volt power input and the other requiring a 3-volt power

input. The available common power, however, might be at a higher level, such as 48V. Converting the 48V common power to the lower levels needed by devices is the job of DC-DC converters. (A3415, left column). In the example with two chips, two different DC-DC converters would be used. (*Id.*)

As the reader no doubt already appreciates, this case will involve extensive use of electrical terminology. Therefore, a brief review of the concepts of electrical *current*, *resistance*, *voltage* and *power* is provided in the next four paragraphs.

Most electrical systems can be analogized to water flowing in a system of pipes. The concept of electrical "*current*", for example, is like the flow rate of water in a pipe. To obtain a flow rate, one can measure the volume of water leaving a pipe during a certain amount of time, and then calculate a rate such as "10 gallons per minute". Similarly, in an electrical system, the flow rate (or "*current*") is related to the number of electrons that flow past a certain point during a certain time period. Electrical current is typically represented by the variable "I". (A4352).

The equivalent to the water pipe in an electrical system is a conductor. A very good conductor of electricity (like a copper wire) is

like a large-diameter water pipe with smooth walls. Water flows easily through such a pipe, and thus the pipe is said to have low "*resistance*" to flow. A poor conductor of electricity (like wood) is like a narrow water pipe packed with sand. It is said to have high "resistance" to flow. Resistance is typically represented with the variable "R".

The "*voltage*" in an electrical system is equivalent to the pressure of water in a pipe. If water is under high pressure in a pipe, opening the end of the pipe will cause the water to shoot out to the lower pressure of the air. Similarly, electrons at a high voltage will tend to flow to a lower voltage. Voltage is usually represented by the variable "V". (A4352). It is also typical to refer to power sources or power requirements by their voltages, such as a "9V battery" or a "12V motor".

Electrical *power* is the amount of electrical *energy* that can be delivered per unit of time. Energy, of course, can be used to do work, like driving a motor, running a computer chip, or lighting an LED. In an electrical system, power is calculated by multiplying the voltage of electricity times its current (VxI). If many electrons are flowing through a conductor (high current) *and* the voltage of those electrons is

high, a very high power is being transmitted. "Power" is typically represented by the variable "P". (A4355).

These concepts can be used to explain a DC-DC converter. DC-DC converters might be used, for example, in a telecommunications facility.[1] Such a facility may have hundreds of computers, lights and motors running, each with their own particular electrical requirements. The telecommunications facility needs to meet these requirements in order for its equipment to run.

Most facilities get power from a power plant over electrical lines. (A3416, left column). These electrical lines typically provide high-voltage, *AC power*. (*Id.*) "AC" stands for "Alternating Current", and must be distinguished from "DC" or "Direct Current". Referring again to the water analogy, DC is like a steady flow of water *in one direction*, at a *constant pressure*. AC, however, is like a back-and-forth flow of water. The water flows in one direction for a time, and then flows backward for a time. While not very useful for gardening, this type of flow can also be used to do work, and has advantages in certain electrical contexts.

[1] Telecommunications is only one of many applications of converter technology.

Many devices in a telecommunications facility, however, require DC power. (*Id.*). To produce DC power, a telecommunications facility will take the incoming AC power, and lower the voltage using a device called a "transformer". After using the transformer, the facility will convert the transformed (lower-voltage) AC power to DC, using a process called "rectification". (*Id.*).

Rectification is an important term for this appeal. Rectification basically involves taking the back-and-forth flow of AC and converting it to the single-direction flow of DC. Using the water analogy, rectification of a back-and-forth flow of water could be accomplished by using a series of floodgates. If the gates are opened and closed at appropriate times, water can be allowed to flow forward and can be precluded from flowing backward. Using a similar "rectification" process involving the electrical equivalent of gates, electrical AC can be converted into electrical DC.

After a rectification process, the facility has converted AC power from the power plant to an internal DC power source operating at some voltage level, often 48V. (*Id.*). This 48V DC source needs to be converted to the kinds of voltage levels required by devices in the

telecommunications facility. (*Id.*; A1184, ¶8). For example, older logic circuits had a requirement for input power at 5V. (A1184, ¶11). To get from 48V to 5V, a DC-DC converter is used. (A36, col. 1, ll. 19-24; A37, col. 4, ll. 6-8). In some cases, one might use a separate DC-DC converter for every different voltage level needed. (A3415, left column). A power system that converts a common supply voltage to different required voltages by using separate DC-DC converters is called a "Distributed Power Architecture" or simply a "DPA". (*Id.*).

DC-DC converters such as the ones used in DPA are the subject of the '190 patent at issue here. (A37, col. 4, ll. 4-12). For example, the first paragraph of the '190 patent Background states:

> "This invention pertains to switching power converters. A specific example of a power converter is a DC-DC power supply that draws 100 watts of power from a 48 volt DC source and converts it to a 5 volt DC output to drive logic circuitry."

(A36, col. 1, ll. 19-24). A DC-DC power converter of the '190 patent is shown conceptually in Fig. 1 of the '190 patent, reproduced here:

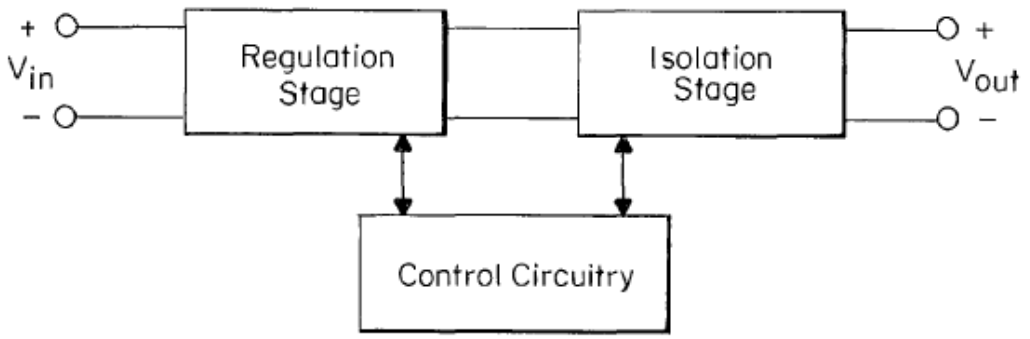


FIG. 1

Figure 1 shows a box-diagram of a DC-DC converter. (A37, col. 4, ll. 33-34). On the left (V_{in}), an input voltage is connected.[2] This might be the common 48V supply of a telecommunications facility, for example. The power that is input to V_{in} flows to the right, passing through circuits that perform functions called "regulation" and "isolation". (*Id.* at ll. 34-38). Some "control circuitry" also guides the overall converter. (*Id.* at ll. 45-47).

The first of the two functions carried out by the '190 patent's DC-DC converter is called "regulation". Note that "regulation" should not be confused with "rectification", discussed above. "Rectification" is the process of turning AC into DC. "*Regulation*", in contrast, is the process of confining a voltage to a particular, nearly constant level. (*Id.* at col.

[2] Note that V_{in} has two connection points, because a voltage is always measured between two points.

4, ll. 23-28). For example, the 48V power source of a facility may not be *exactly* 48V. Instead, it might vary randomly over a range (*e.g.* 45-51 V). This variation could be detrimental to the system. The DC-DC converter thus uses regulation to reduce the variation. (*Id.*) At the output of the regulation circuitry (just before isolation), for example, the variation might be reduced to 47.9 - 48.1V.

The second function carried out by the DC-DC converter is called "isolation". In the "isolation" function, the voltage is lowered (e.g.) from 48V to 5V, while hopefully maintaining the same overall power. (*Id.* at col. 4, ll. 9-12 and 37-38).

How does the converter manage to lower the voltage but keep the power level the same? Here, the converter uses a technique that has been known for more than a century: the DC power is converted back to a form of AC power.[3] (A38, col. 5, ll. 13-36). AC power has the advantage of being easily convertible between voltage levels using a transformer.[4] In this way, the AC power's voltage is lowered to the

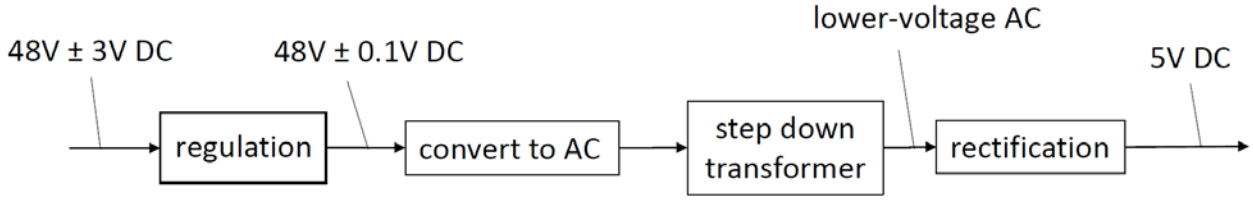
[3] The waveform of the power may not look like the typical sinusoidal AC power. The point is that the current is changing, and this allows a transformer to be used.

[4] It is this fact that led to the use of AC power in power lines in the 1880s. *See, e.g.*, http://www.teslasociety.com/ac.htm.

appropriate level (A37, col. 4, ll. 9-12; A4378), and then the lower-voltage AC power is converted back to DC. So the "isolation" circuitry carries out the following process: DC → AC (high voltage) → AC (low voltage) → DC. The circuit is said to be "isolating", because there is no direct electrical connection from one side to the other. (A4378). Rather, energy is transmitted across the transformer using magnetic field fluctuations. (A4378).

The process of converting the low-voltage AC back to DC is carried out using a *rectification* system. As previously explained, the rectification system gates the forward and backward flows of current, so that they end up flowing in the same direction at the output.

After the step of rectification, a total DC-DC voltage conversion is accomplished. The overall conversion process described in the '190 patent looks something like this (using the 48V-5V example of the patent):



The technical disclosure of the '190 patent claims to provide an improvement in the last box ("rectification") on the right-hand side.

(A36, col. 1, l. 65 – col. 2, l. 3). In the prior art, there were basically[5] two known categories of rectification circuits. (A1433, upper left). The first category used *diode rectifiers*. Diodes are electrical devices that, in most circumstances, only allow electrical current to flow in one direction. One could thus set up a system of diodes that would conduct forward AC power in the right direction, at the right time, resulting in a rectified (DC) output.

Diode rectifiers exacted a toll, however. (A36, col. 1, ll. 39-42). Specifically, diodes had a forward voltage drop. Current passing through the forward voltage drop of a diode would experience a loss of energy. (*Id.*) Energy was converted to heat, and thus wasted.

A second form of rectification circuit replaced diodes with *transistors*. (*Id.*, col. 1, ll. 42-47; A1433, upper left). The preferred transistor was a MOSFET ("Metal Oxide Semiconductor Field Effect Transistor"). (*Id.*). Unlike a diode, a MOSFET allowed current to flow in both directions. (A4367). However, a MOSFET needed to be turned ON and OFF by supplying the correct electrical signals to it. When ON, a MOSFET allowed current flow, and when OFF, no current flow was

[5] This description is simplified, but is sufficiently accurate for purposes of this appeal.

allowed in the reverse direction. So, by turning MOSFETs ON and OFF at the right times, it was also possible to construct gates that would rectify AC to DC. Such MOSFET rectifiers had no forward voltage drop and low resistances, and thus conserved power compared to diodes. (A4367). Because the MOSFETs had to be turned ON and OFF (controlled), they were called "*controlled* rectifiers" in the language of the '190 patent. (A1183-1184, ¶6). The patent and prior art also use the equivalent term "synchronous rectifiers" (e.g., A61, col. 4, ll. 58-60), which denotes the fact that the MOSFETs have to be turned ON and OFF at the right *time* in order for rectification to occur. (A1466). Rectification using MOSFETs is called "synchronous rectification".

The '190 patent purports to provide an improvement to known synchronous rectification techniques. (A36, col 1, l. 65- col. 2, l. 3). The '190 patent states in its Background that:

> "In order to reduce [diode-based] conduction loss, **the diodes are sometimes replaced with transistors whose on-state voltages are much smaller**. These transistors, called synchronous rectifiers, are **typically power MOSFETs**.... **The use of transistors** as synchronous rectifiers in high switching frequency converters **presents several technical challenges**."

(A36, col. 1, ll. 38-57) (emphases added). The '190 patent, while recognizing the prior art use of synchronous rectifiers, purported to provide an improvement:

> "Various approaches to addressing these technical challenges have been presented in the prior art, but **further improvements are needed**. In response to this need, **a new power circuit topology designed to work with synchronous rectifiers in a manner that better addresses the challenges is presented here**."

(A36, col. 1, l. 65- col. 2, l. 3) (emphases added).

2). History of the '190 patent

The '190 patent issued from a chain of applications. The first such application was filed by Dr. Martin Schlecht, named inventor and CEO of the Appellee, SynQor, in 1997. (A27). Following four intervening continuation and divisional applications, the '190 patent issued in 2006. (*Id.*).

Around the time of his provisional application (1997), Dr. Schlecht founded SynQor. (A1189, ¶4). SynQor set about the business of making DC-DC converters, of the type described in the '190 patent disclosure. (A1189, ¶5). These converters had a single housing containing a

regulation stage and an isolation stage, as shown in Fig. 1 of the '190 patent. As Dr. Schlecht testified in the *Artesyn* litigation:

> "The claims in this patent [the earliest patent in the family][6] are directed to the kinds of circuits and designs and so on that we use in SynQor's very first products, the ones that I'm talking about here, products that both isolated and regulated all in one product."

(A2508, 25:9-13). Such converters will be referred to as DPA "brick" converters in this brief. "DPA" stands for "Distributed Power Architecture". (A3451). SynQor continued producing only DPA brick converters until around 2002, or nearly five years after its original filing. (A4309).

Around the year 2000, however, SynQor appears to have noticed a change in the industry. When SynQor discussed products with its customers, some customers no longer wanted SynQor's DPA "brick" products. Instead, customers began to ask for another stage of down-conversion. (A3160). A customer might request to convert from 48V to 12V, use the 12V to distribute power across a power bus to various

[6] U.S. Pat. No. 5,999,417.

places, and then convert from 12V down to levels needed by specific components (e.g. 5V).

This sort of power distribution architecture became known as "Intermediate Bus Architecture", or simply "IBA". (A3416). IBA would eventually grow in popularity for some applications versus the more traditional DPA. (*Id.*).

Much of SynQor's argument is based on its contention that Dr. Schlecht invented IBA. (*e.g.* A698). Thus, an understanding of the meaning of IBA (as compared, say, to DPA) is important for the resolution of this appeal. A good comparison between IBA and DPA is shown in a 2003 article by Bob White—an employee of a third party—entitled "Emerging On-Board Power Architectures". (A3414-A3419).

Figure 1 of the White article shows a typical DPA approach, where the power from the main 48 V ("front-end") supply (left side) is routed over a distribution bus to three different logic boards. (A3415-3416). On each logic board, there are multiple DPA brick converters (shown as boxes) used to produce various voltage levels (V1, V2, V3). (A3415). Figure 1 of the White article is shown here:

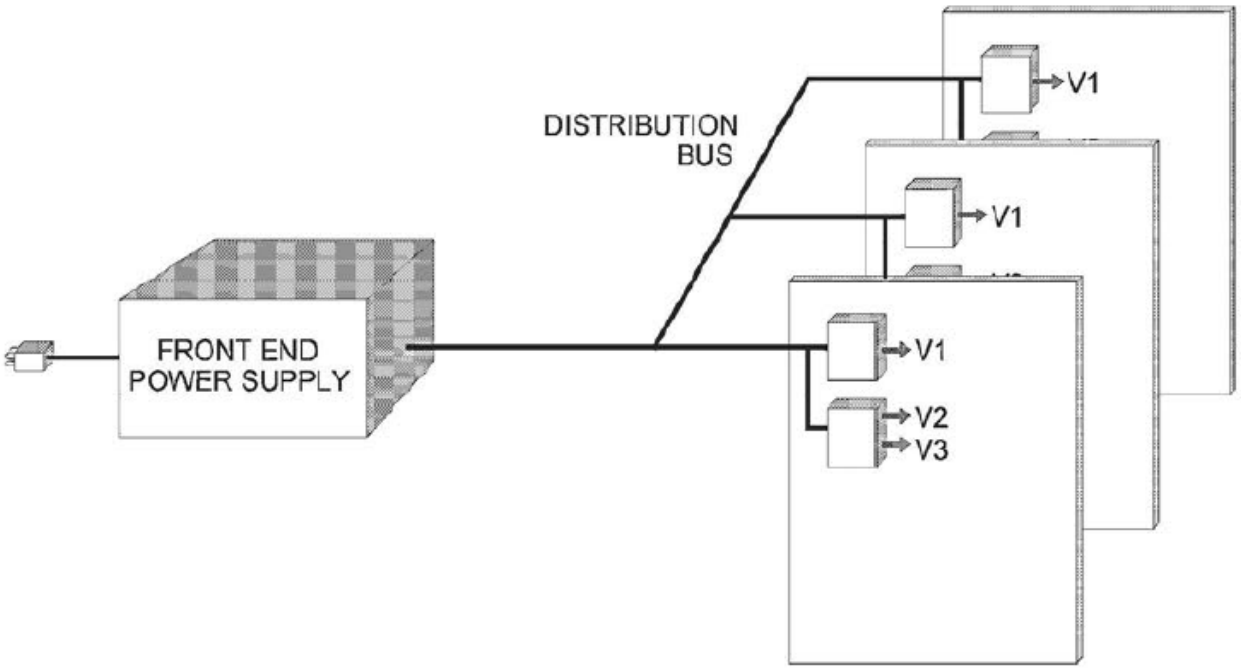


Figure 1. Traditional Distributed Power System

The Intermediate Bus Architecture, however, adds another converter ("bus converter") on the distribution bus. (A3416-A3417). This effectively divides the bus into two busses, with each bus having a different voltage. (A3417). For example, the first distribution bus might be at 48V, while the second distribution bus is at 12V. The result is shown in Figure 2 of White's article:

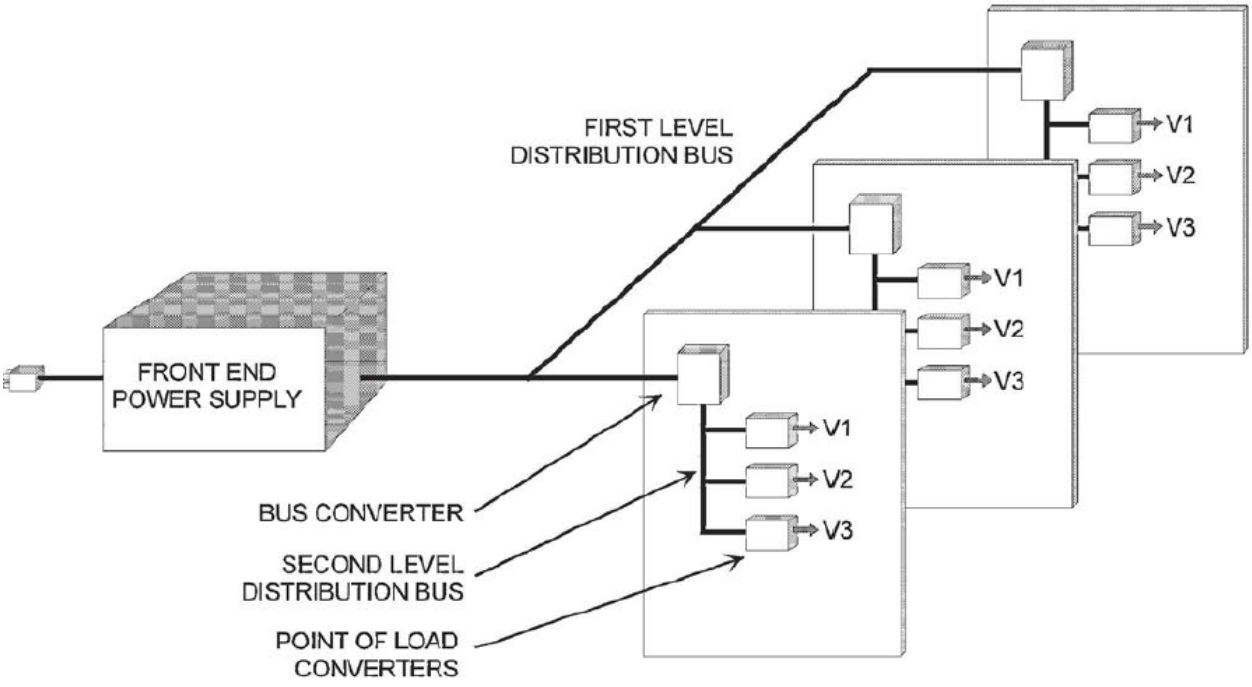


Figure 2. Two Level Distributed Power System (Intermediate Bus Architecture)

In Figure 2, a "bus converter" has been added in the distribution bus. This results in a "second level distribution bus" (also known as an "intermediate bus"). (A3416-3417). The electrical output of the "bus converter" is transmitted by this intermediate bus across the board to a number of "point of load" converters, or simply "POLs". (A3416-A3417). The POLs contain the regulation circuitry. (A3417). The isolation stage, however, comes earlier, in the "bus converter". (*Id.*). The bus converter and POLs are separate units. (A3416-3417). This is unlike the converters described in the principal embodiments of the '190 patent, which have a single regulation stage first, followed by a single isolation stage, "all in one product". (A2508, 25:9-13).

In the 2002-2005 timeframe, a number of companies began offering products directed at IBA. (A1549; A3416). SynQor was apparently aware of these developments, but not entirely convinced of the value of IBA versus the more traditional DPA. For example, a SynQor product roadmap from December, 2002 states that designers should consider using a bus converter where "costs of designing and implementing POL nonisolated converters are less than standard brick solution". (A3241). Two years later, in 2004 (seven years after Dr. Schlecht's original application was filed), Dr. Schlecht published an article comparing the relative merits of DPA and IBA. (A3451-3453). That article begins as follows:

> "Intermediate Bus Architecture (IBA) or traditional Distributed Power Architecture (DPA), which one do you choose? It would be nice if one approach were so much better than the other that you could answer this question definitively for all scenarios. But that is not the case. Instead, often the two approaches are quite close to each other in performance, and even the definition of 'better' is at best complex."

A3451. It was not until 2005 that SynQor sought to target the concept of IBA in its patent claims. In June of 2005, eight years after

its original patent filing, SynQor went back to the USPTO, where it still had continuations pending. In the application leading to the '190 patent, SynQor canceled claims directed to the principal embodiments. SynQor's replacement claims were aimed at capturing the IBA architecture it had seen develop over the preceding five years.[7] SynQor based this change on four lines in column 14 of the '190 patent, which read:

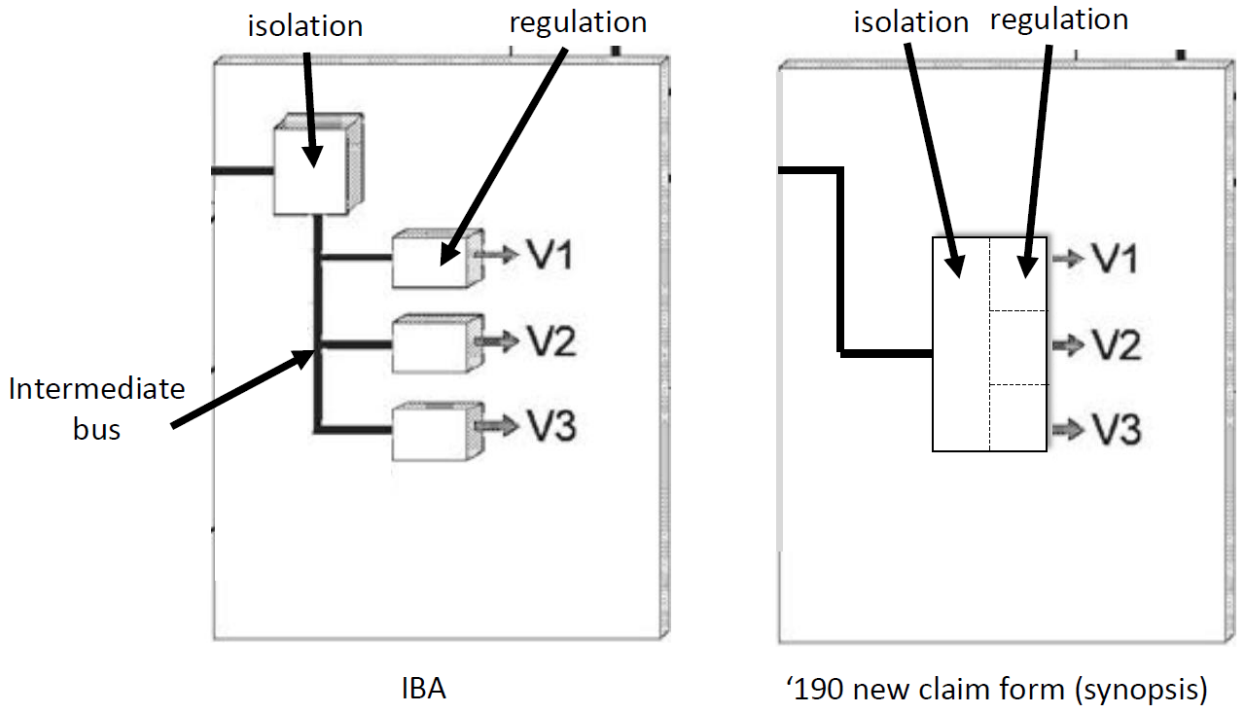
> "It is also possible to use DC-DC switching regulators on the secondary side to achieve the additional regulation desired, or to create more than one output voltage from any of the outputs of the isolation stage."

(A42, col. 14, ll. 36-39). The June 2005 amendment caused the claims to take on the form they have now, where a first "non-regulating isolation stage" feeds "a plurality of non-isolating regulation stages". (A44).

SynQor had no basis in the specification, however, to claim an intermediate bus between isolation and regulation stages, and left this core component of IBA out of the claims. This difference between IBA and SynQor's claims as amended in 2005 is shown in the following

[7] *See* U.S. App. Ser. No. 10/812,314, Amendment of June 13, 2005.

diagram, which has been adapted by Vicor from Figure 2 of the White 2003 paper:



The diagram on the left represents a form of IBA, which has a bus converter that feeds a bus, which in turn feeds multiple POLs. (A3416-A3417). The diagram on the right summarizes the flow of SynQor's amended claims based on the statement in column 14 of the '190 patent.[8] At most, the statement in column 14 allowed SynQor to argue for reversing the order of isolation and regulation and for adding multiple

[8] This diagram shows the ordering and connection of stages, but does not show claim elements within those stages.

regulation stages (compare the '190 patent, Fig. 1). Nowhere, however, did the specification disclose the element of the intermediate bus.

The '190 patent and its re-directed claims issued in 2006. A27. In 2007, SynQor began suing industry members in the United States District Court for the Eastern District of Texas.

3). SynQor's East Texas lawsuits and concurrent reexaminations.

SynQor first filed suit in East Texas against a number of third parties for infringement of the '190 patent in *SynQor, Inc. v. Artesyn Techs., Inc. et al.*, Case No. 2:07-CV-497 (E.D. Tex.). This will be referred to as the "*Artesyn* litigation". SynQor obtained a jury verdict against the third parties in the *Artesyn* litigation. (A4436). The denial of the defendants' motion for JMOL was affirmed by this Court in *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365 (Fed. Cir. 2013).

One of the defendants in the *Artesyn* litigation, Murata Manufacturing ("Murata") initiated an *inter partes* reexamination against the same '190 patent at issue here, on August 19, 2009.[9] The assigned Examiner issued a final rejection of the claims on September 28, 2011. SynQor appealed to the PTAB.

[9] *Inter partes* reexamination control number 95/001207.

After the jury verdict in the *Artesyn* litigation, Murata filed a mandamus petition against the USPTO, alleging that the PTAB had failed to comply with its statutory mandate to conduct reexams with "special dispatch".[10] Murata and the USPTO agreed to dismiss the mandamus action. Shortly thereafter, the PTAB issued a decision against Murata, reversing the Examiner's decision.[11] Murata did not appeal to this Court.

After the jury verdict in the *Artesyn* litigation, Vicor filed (2011) a Declaratory Judgment action in Massachusetts, and SynQor filed suit against Vicor and two additional defendants in the Eastern District of Texas. Vicor then filed its own request for *inter partes* reexamination of the '190 patent on September 8, 2011, resulting in the present proceeding. The assigned Examiner (different from the Examiner in the Murata reexam) again issued a final rejection of all claims of the '190 patent on November 26, 2012. (A2). SynQor appealed. (*Id.*). The PTAB again reversed the Examiner (A3), despite vast differences in the record as compared with the Murata reexamination. Vicor then appealed to this Court.

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[10] *See* Petition for Writ of Mandamus at ¶32 *Murata Mfg., Co., Ltd. v. Rea*, No. 1:13-cv-00742 (E.D. Va. Filed June 19, 2013).

[11] *Murata Mfg. Co., Ltd. v. SynQor, Inc.*, PTAB Appeal No. 2012-012209, 2013 Pat. App. LEXIS 5715 (Aug. 19, 2013).

SUMMARY OF THE ARGUMENT

The PTAB erred by reversing the Examiner. The Examiner rejected certain claims as anticipated over U.S. Pat. No. 5,377,090 to Steigerwald ("S'090"). The only claim elements alleged to be missing from S'090 itself were those related to "controlled rectifiers". S'090 uses *diode rectifiers* instead. However, S'090 incorporates by reference U.S. Pat. No. 5,274,539, also to Steigerwald ("S'539"). S'539 expressly teaches that controlled rectifiers can be substituted for diode rectifiers. The PTAB, however, found this teaching *unrelated* to S'090.

The PTAB's conclusion applied the governing law incorrectly and is unsupported by substantial evidence. S'090 has only one embodiment, and expressly states that S'539 is related. Moreover, the substitution in S'539 applies to all embodiments of S'539. The circuit to which the substitution applies is the *same circuit*—with the same figure and text description—in both patents. The PTAB furthermore erred by applying an obviousness standard to an anticipation rejection, and by probing the *timing* of the incorporation-by-reference, thereby erroneously holding that earlier-made statements could not modify later-made statements. Such a decision would preclude almost any use of incorporation-by-

reference. The PTAB's decision should be reversed. Similarly, the PTAB's reversal of obviousness grounds (S'090 in view of Cobos and/or Pressman) based on its findings regarding S'090 / S'539 should be reversed.

The PTAB further erred in its analysis of obviousness of claims 24-26 over S'090 / S'539. Specifically, the PTAB erroneously confused the term "synchronous rectifiers" with the similar-sounding term "switching regulators", causing the PTAB to apply a claim limitation not present in claims 24-26. The PTAB further erred by finding facts relating to commercial success that were clearly not based on substantial evidence, and by approaching the commercial success analysis in a formulaic, inflexible manner. This caused the PTAB to overlook extensive objective evidence that the claims are obvious. The PTAB's decision here should be vacated and remanded.

Lastly, the PTAB erred by reversing the Examiner's rejection of claims 1-38 over the Cobos and Pressman references. The PTAB *made the same fact findings put forward by Vicor in its request for reexamination* concerning motivation to combine. These findings were relied on by the Examiner in support of a motivation to combine.

Among other things, the PTAB concluded that Pressman taught a way to provide multiple outputs at high efficiency. After making the same underlying fact findings as the Examiner, the PTAB then inexplicably concluded that the Examiner's rejection was based on hindsight. The PTAB also erred in its findings and approach to commercial success, as described above. The PTAB's decision on this issue should likewise be vacated and remanded.

ARGUMENT

A. STANDARD OF REVIEW

1). General

This Court reviews the PTAB's "compliance with governing legal standards de novo and its underlying factual determinations for substantial evidence." *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2012).

This Court "must judge the propriety of [an agency's] action solely by the grounds invoked by the agency." *SEC v. Chenery Corp.*, 332 U.S. 194, 196 (1946). These grounds "must be set forth with such clarity as to be understandable." *Id.* at 196-97.

2). Anticipation

Anticipation is a question of fact reviewed for substantial evidence. *See In re Baxter Travenol Labs*, 952 F.2d 388, 390 (Fed. Cir. 1991).

3). Incorporation-by-reference

Whether a reference is incorporated-by-reference is a question of law that is reviewed *de novo*. *See Advanced Display Sys. v. Kent State Univ.*, 212 F.3d 1272, 1283 (Fed. Cir. 2000). Findings concerning the

teachings of the unified reference are reviewed for substantial evidence. *See id.*

4). Obviousness

Obviousness is a question of law, reviewed *de novo*. *See Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2012). The analysis is supported by facts that are reviewed for substantial evidence. *See id.*

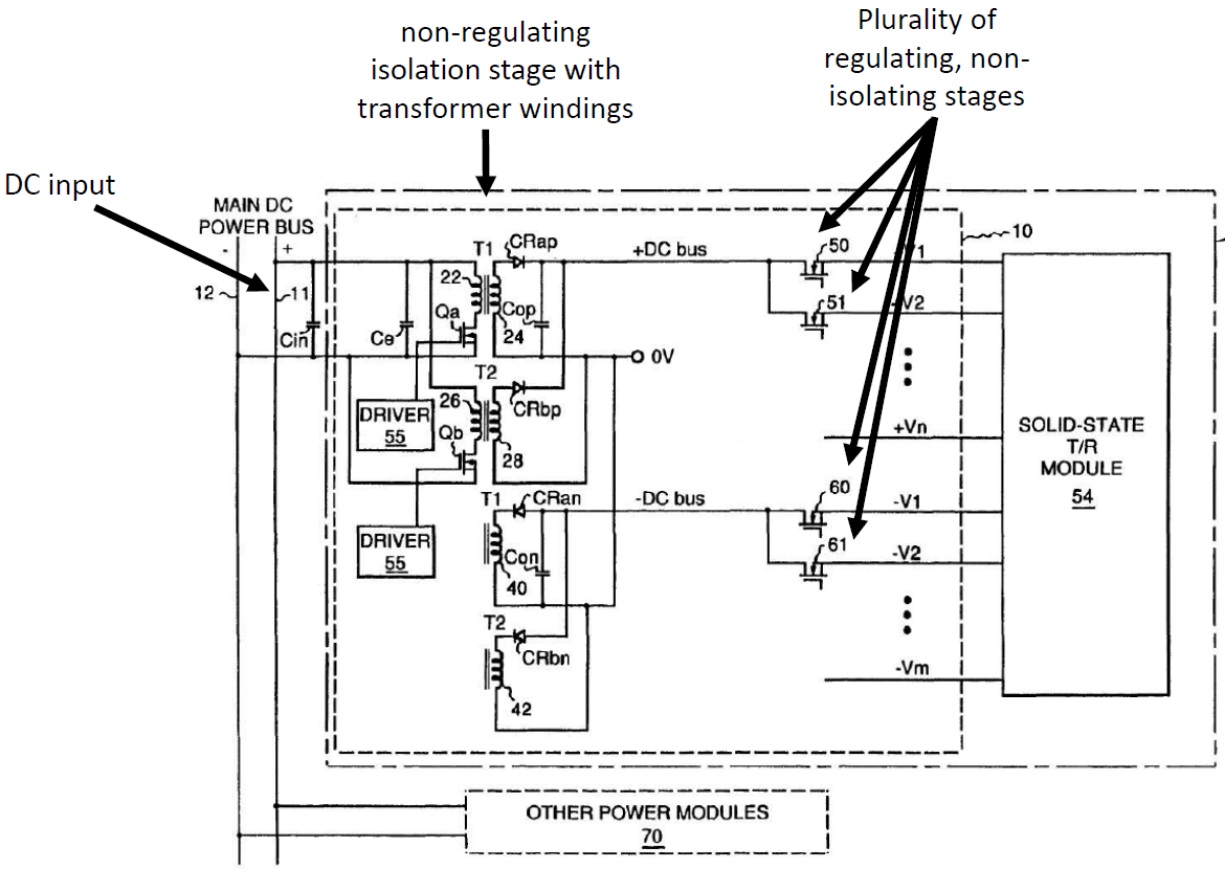
B. DISCUSSION

1). The PTAB erred by reversing the Examiner's finding that Steigerwald '090/'539 anticipates claims 20-23, 27, 29, 30, 32 and 33.

The Examiner below found that Steigerwald '090/'539 anticipates claims 20-23, 27, 29, 30, 32 and 33 of the '190 patent. The PTAB erred by reversing the Examiner.

Steigerwald '090 (hereinafter "**S'090**")[12] teaches an intermediate bus architecture in the form of a single embodiment, shown in Fig. 1. (A65). There appears to be no dispute that the single embodiment of S'090 teaches all elements of applicable claims, except for those related to the use of controlled rectifiers. (A7-A9). Figure 1 of S'090 is shown below, with the main elements of independent claim 20 labeled by Vicor:

[12] U.S. Pat. No. 5,377,090 (A64-A68).



S'090 is missing only one portion of the isolation stage. Instead of *controlled rectifiers*, the embodiment of S'090 uses *diode rectifiers* (shown as CRap and CRbp in Fig. 1, above). (A66 col. 2, ll. 29-32). S'090, however, incorporates Steigerwald '539 (hereinafter "**S'539**")[13] by reference. (A66, col. 1, ll. 7-9). S'539 expressly teaches that *synchronous rectifiers* (aka "controlled rectifiers") can be used in place of *diode rectifiers*. Specifically, S'539 states:

[13] U.S. Pat. No. 5,274,539 (A49-A63).

> "**In other alternative embodiments**, **such as** those of FIGS. 7-9, **synchronous rectifiers** SRa and SRb **are used instead of diodes** CRa and CRb of FIGS. 4 and 6."

(A61, col. 4, ll. 58-60) (emphasis added).

The above-quoted statement in S'539 will be referred to herein as the "alternative embodiments" statement. The statement expressly applies to Figures 4 and 6 of S'539. (*Id.*). After substituting in the controlled rectifiers, the statement expressly results in Figs. 7-9 of S'539. (*Id.*). Note, however, that the statement is broadly worded, and not bound to specific figures ("alternative embodiments, **such as** those of FIGS. 7-9…"). (*Id.*).

The correctness of the PTAB's decision turns on how the "alternative embodiments" teaching in S'539 relates to the sole embodiment of S'090. Vicor contends—and the Examiner agreed—that the "alternative embodiments" statement of S'539 does apply to the sole embodiment in S'090. (A1014-A1017). S'090 expressly states that S'539 is related. Furthermore, the "alternative embodiments" statement in S'539 applies to *all embodiments* of S'539, and S'090 has *only one embodiment*. That single embodiment uses the *same rectification circuit* (down to the reference numerals) as Fig. 4 of S'539, to which the

"alternative embodiments" statement expressly applied. The text description of that circuit in the two patents is also virtually identical.

The PTAB, however, held otherwise. (A7-A9). To support its holding, the PTAB made several findings concerning the relationship of "alternative embodiments" in S'539 to the sole embodiment of S'090. (*Id.*). Each of the findings is either based on an incorrect application of law or is unsupported by substantial evidence (or both).

Most importantly, the PTAB found that S'539's "alternative embodiments" teaching was directed to a "discrete embodiment" in S'539, and that this "discrete embodiment" was unrelated to the sole embodiment in S'090. In the PTAB's words:

> "Requester has taken the isolated teaching of a discrete embodiment of Steigerwald '539 exchanging a MOSFET for a diode, and modified it with description from a different embodiment from Steigerwald '090, without an express or even implied disclosure of this modification."

(A9). The PTAB's finding that S'539's "alternative embodiments" statement was unrelated to S'090's lone embodiment is unsupported by substantial evidence. The first problem with the PTAB's finding is that

S'090 *actually says* that S'539 is related. The first paragraph of S'090 states:

> "[t]his application **is related** to commonly assigned U.S. Pat. No. 5,274,**539** of R.L. Steigerwald….".

(A66, col. 1, ll. 7-9). This sentence, of course, refers to *all of* the S'539 patent (not a specific embodiment or teaching), but that fact is irrelevant here. It is irrelevant because the "alternative embodiments" statement in S'539 applies to *all embodiments* of S'539.[14] Furthermore, S'090 has *only one* embodiment. (A64-A68). If a statement that applies to *all embodiments* of S'539 is **un**related to the *only* embodiment in S'090—as the PTAB found—then logically the two patents cannot be related at all. This is clearly inconsistent with S'090's statement that the two patents are, in fact, related. (A66, col. 1, ll. 7-9).

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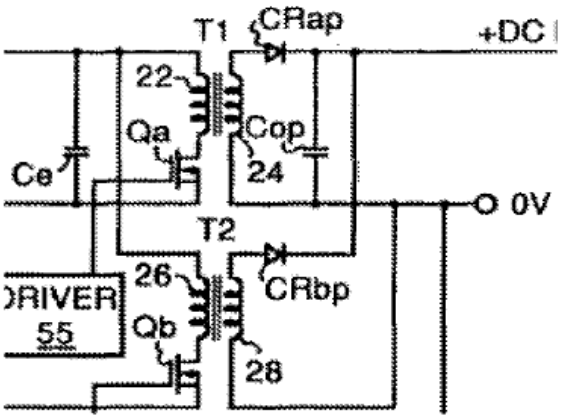
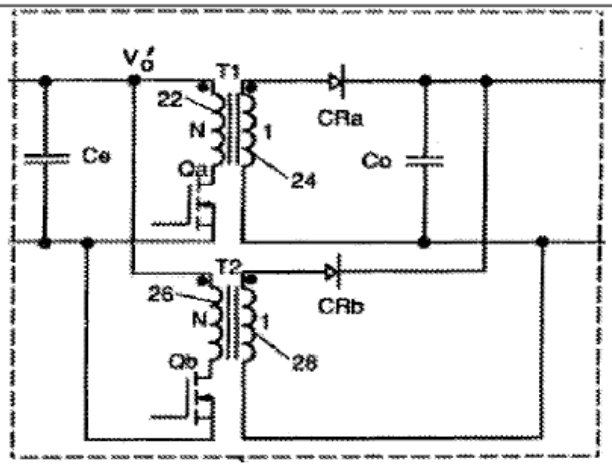
[14] There are two main converters in S'539, represented by Figs. 4 and 6. (A61 col. 3, l. 14 – col. 4, l. 55). Figs. 1-3 represent the prior art (A60-61, col. 2, l. 46 – col. 3, l. 13), and Fig. 5 is a larger system that uses one of Fig. 4 or Fig. 6. (A61, col. 4, ll. 28-37). The "alternative embodiments" statement expressly includes both Fig. 4 and Fig. 6 (and thus indirectly Fig. 5). (A61, col. 4, ll. 58-60). Figures 7-9 represent the embodiments with controlled rectifiers (after replacement of diode rectifiers with controlled rectifiers). (*Id.*) Fig. 10 shows waveforms of Figs. 7-9. (A62, col. 5, ll. 19-42). Thus, the "alternative embodiments" statement applies to all embodiments of S'539.

The second problem with the PTAB's reasoning is that S'090 uses *the same rectification circuit* as the Figure 4 embodiment of S'539, to which the "alternative embodiments" statement expressly applies. (A61, col. 4, ll. 58-60). The relevant portions of circuits shown in Fig. 1 of S'090 and Fig. 4 of S'539 are virtually identical, down to the reference numerals. A side-by-side comparison is shown below:



Steigerwald '090, Fig. 1 excerpt



Steigerwald '539, Fig. 4 excerpt

(A65 and A53). The S'090 circuit has a capacitor Ce at its input (left side), just like capacitor Ce in Fig. 4 of S'539. Figure 1 of S'090 has two transformers T1 (RN 24) and T2 (RN 26), just like transformers T1 (RN 24) and T2 (RN 26) of Fig. 4 of S'539. Driving the two transformers in S'090 Fig. 1 are transistors Qa and Qb, just like transistors Qa and Qb of Fig. 4 of S'539. Each of the transformers in Fig. 1 of S'090 has a diode rectifier

(CRap and CRbp) at its output, just like the diode rectifiers CRa and CRb at the output of the transformers of Fig. 4 of S'539. The diode rectifiers are biased in the same direction (as indicated by the arrows). *It is these diode rectifiers to which the "alternative embodiments" statement in S'539 applies.* Furthermore, transformers T1 and T2 in Fig. 1 of S'090 have an output capacitor Cop, just like the output capacitor Co of Fig. 4 of S'539. In both patents, the outputs of both transformers are wired in parallel.

The identity of the relevant circuit is confirmed by the texts describing the circuit in both patents, which are nearly identical. (*Compare* A66 col. 2, ll. 14-30 *with* A61, col. 3, ll. 14-32). The relevant portions of the specifications are shown side-by-side below:

As shown in FIG. **1**, power is provided to a power module **10** via power buses **11** and **12**. The power module includes a capacitance-multiplying converter **20** which comprises a series combination of a first switching device Qa and a primary winding **22** of a first transformer **T1** coupled in parallel with an energy-storage capacitor Ce. A secondary winding **24** of transformer **T1** is coupled in parallel, via a diode rectifier CRap, to a small high-frequency output filter capacitor Cop. Capacitance-multiplying converter **20** further includes a series combination of a second switching device Qb and a primary winding **26** of a second transformer T2 also coupled in parallel with energy-storage capacitor Ce. Switching devices Qa and Qb are illustrated as FET's; however, any suitable types of switching devices may be used. A secondary winding **28** of trans-	**FIG. 4** illustrates a power system employing a capacitance-multiplying converter **20** in accordance with the present invention. Capacitance-multiplying converter **20** includes a series combination of a first switching device Qa and a primary winding **22** of a first transformer **T1** coupled in parallel with an energy-storage capacitor C_e. A secondary winding **24** of transformer **T1** is coupled in parallel, via a diode rectifier CRa, to a small high-frequency output filter capacitor Co. Capacitance-multiplying converter **20** further includes a series combination of a second switching device Qb and a primary winding **26** of a second transformer **T2** also coupled in parallel with energy-storage capacitor Ce. A secondary winding **28** of transformer **T2** is coupled in parallel, via a diode rectifier CRb, to output filter capacitor Co. Transformers **T1** and **T2** have substantially the same turns ratio N. Switching devices Qa and Qb are illustrated as FET's; however, any suitable types of switching devices may be used.
S'090 description (A66, col. 2, ll. 14-30).	S'539 description (A61, col. 3, ll. 14-32).

It is inconceivable that a person of ordinary skill in the art would not recognize the relationship between Fig. 4 of S'539 and the lone embodiment of S'090. As the reexamination Examiner found:

> "Steigerwald '539 is not a series of 'various documents', it is a patent with only five columns of technical disclosure. It is also very clearly a predecessor to Steigerwald '090. Despite the Patent Owner's protestations, Steigerwald '539 is entirely directed to the same kinds of 'capacitance multiplying' power converters referenced in the Steigerwald '090 patent. This is demonstrated, most obviously, by the fact that Steigerwald '090 expressly stated that the '539 patent is related to the 090 patent (See Steigerwald '090, col. 1, 11. 7-8). Moreover, the isolation stage of the two patents is nearly identical, down to the reference numerals….[figure comparison omitted]….The text describing the isolation stage Figure is also nearly identical between the two patents (Compare '090 patent, col. 2, 11. 14-32 with '530 patent, col. 3, 11. 14-32). Based on this, it is eminently reasonable to believe that a person of ordinary skill in the art would see exactly how the converters of the '539 patent relate to the converter of the '090 patent."

(A778-A779).[15] The PTAB did not address these direct links between the lone embodiment of S'090 and the Figure 4 embodiment of S'539. (A7-A9). Instead, the PTAB offered two independent reasons for finding that the controlled rectifier embodiments of S'539 were unrelated to S'090. In the PTAB's words:

> "We are in agreement with the position of the Patent Owner, that: '[t]he assertion that Steigerwald '539 sets up an alternative embodiment as a modification to Steigerwald '090, Fig. 1 is contrary to the express purpose of both patents: which is primarily to supply the energy pulse for a radar T/R module (illustrated in Steigerwald '539, Fig. 2). The ordinary artisan could not reasonably conceive that the text of the Steigerwald '539 Patent could modify the later-filed Steigerwald '090 as asserted.'"

(A9). The PTAB's two reasons apply incorrect law and are unsupported by substantial evidence. The PTAB first reasons that, if the statement about "alternative embodiments" in S'539 were to apply to S'090, it would be "contrary to the express purpose of both patents". (*Id.*). The PTAB provided no further explanation. (*Id.*). The most

[15] For similar reasons, the S'090 patent properly incorporates the S'539 by reference.

likely interpretation of the PTAB's (cryptic) statement concerning the "purpose" of the references is that the PTAB is applying a teaching away doctrine. If true, this would be legal error in the context of an anticipation challenge. As this Court held in *Krippelz v. Ford Motor Co.*:

> "Finally, the court cited testimony from Mr. Krippelz's expert that a conical beam of light **'probably wouldn't be a very effective way to accomplish the purpose of DuBois**,' and from that reasoned that the jury could reasonably have held that DuBois 'actually teaches away from using a beam.' [record cite omitted]. First and foremost,[5] **teaching away is not relevant to an anticipation analysis**; it is only a component of an obviousness analysis."

667 F.3d 1261, 1269 (Fed. Cir. 2012) (emphasis added).

Even if Steigerwald's "purpose" were relevant, the conclusion drawn by the PTAB is unsupported by substantial evidence. This is because S'539 *expressly teaches* substituting controlled rectifiers for diodes. (A61, col. 4, ll. 58-60). And as found by the PTAB, S'539 has the *same purpose* as S'090. (A9). If the purpose of the two references is the

same, and one reference teaches the substitution, the same substitution in the other reference would be *more apparent*—not less.

Furthermore, if one were to take the purpose of the Steigerwald references into account, one might also take into account Dr. Steigerwald's testimony about what a person of ordinary skill would have understood about that purpose. Dr. Steigerwald is a third-party witness, not retained by either Vicor or SynQor.[16] When asked about the relationship between S'539 and S'090 in deposition, Dr. Steigerwald testified as follows:

> "**Q.** Did you consider, umm, the 090 Patent disclosure to be an extension on the circuit designs that were disclosed in the 539 Patent?
> **A.** Yes."
>
> (A2123, l. 25 - A2124, l. 5).
>
> ...
>
> "**Q.** Would a person, reading your 090 Patent together with your 539 Patent, who was a skilled power electronics designer, have understood that the teaching of the 539

[16] A2068, l. 22 – A2070, l. 13. Dr. Steigerwald was examined by both sides (A2066, ll. 5-7), and has more than thirty years of experience in power electronics. (A2073, l. 12 – A2076, l. 17).

> Patent to replace diodes with synchronous rectifiers was equally applicable to the circuit disclosed in the 090 Patent?
>
> **A.** I believe so."

(A2129, ll. 17-24).

The PTAB's second reason for finding that the "alternative embodiments" statement was inapplicable to S'090 was that:

> "The ordinary artisan could not reasonably conceive that the text of the Steigerwald '539 Patent could modify the **later-filed** Steigerwald '090 as asserted.'"

(A9) (emphasis added). This appears to be a finding about the *timing* of S'539's disclosure relative to that of S'090. The PTAB appears to be saying that *earlier* statements in S'539 could not modify the *later* disclosure of S'090.

This finding is both legally erroneous and unsupported by substantial evidence. It is legally erroneous because incorporation-by-reference doctrine prohibits inquiry into the relative timing of the disclosures. Instead, the PTAB was required to first determine whether there was incorporation, and then to *treat the references as a single*

document when considering anticipation. As held by this Court in *Advanced Display*:

> "[T]he court's role is to determine what material in addition to the host document constitutes the single reference. The factfinder's role, in turn, is to **determine whether that single reference describes the claimed invention**."

Advanced Display, 212 F.3d at 1283 (emphasis added). The PTAB cites no authority directing the factfinder to probe the "when" and "how" of incorporation in determining whether the unified document anticipates the claims. (A9). Indeed, holding that earlier-made statements cannot affect a later-made disclosure would vitiate the incorporation-by-reference doctrine, as *most* incorporated references precede their incorporating references.

The PTAB's decision was legally erroneous for another reason: this Court's precedent makes clear that *statements of alternative* in an earlier, incorporated reference *can* modify embodiments in the later, incorporating reference. For example, in *Ultradent Prods. v. Life-Like Cosmetics*,[17] the incorporating reference (Munro) taught an apparatus for bleaching teeth, but not a bleaching composition. *See id.* at 1068. Munro, however, referred

[17] 127 F.3d 1065, 1068 (1997).

to the Proxigel bleaching agent, and incorporated the Rosenthal patent. *See id.* The Rosenthal patent disclosed the composition of Proxigel and several alternative ingredients. *See id.* The teaching of one of the alternative ingredients (slightly acidic vinyl polymer with active carboxyl groups) was necessary to anticipate. *See id.* This Court reversed summary judgment of no anticipation, finding:

> "Although Rosenthal states that a neutralized salt of carboxypolymethylene is the preferred form of the polymer, the disclosure of Rosenthal is not limited to the neutralized salt. Rather, the patent refers to carboxypolymethylene in general as the thickening agent for the claimed composition. The district court thus erred by construing the scope of the Rosenthal disclosure as limited to the preferred embodiment."

Ultradent, 127 F.3d at 1068.

Similarly, in *Callaway Golf Co. v. Acushnet Co.*,[18] this Court reversed summary judgment of no anticipation. In so doing, the court held that a statement in the incorporated reference (Molitor) that "[m]ixtures of the above described material may also be used" would lead to mixtures being

[18] 576 F.3d 1331 (Fed. Cir. 2009).

used in the later, incorporating reference (Nesbitt). *See id.* at 1347 and 1345-46.

The PTAB's reasoning is further unsupported by substantial evidence, because the PTAB focuses on the *act of making the statement* in the disclosure of S'539 (performed at an earlier time), thereby ignoring the *act of incorporation* (performed at a later time). Through the act of incorporation, the inventors of S'090 adopted the content of their own S'539, with full knowledge of its "alternative embodiments" teaching. This renders moot any objection based on the relative timing of the two original disclosures.

The PTAB's overall holding also directly contradicts the PTAB's reasoning concerning S'090 and S'539 in a prior case.[19] In prior *inter partes* reexamination 95/001207 (initiated by non-party Murata and directed to the '190 patent at issue here), the PTAB considered a combination of S'090 and Cobos.[20] SynQor objected to the combination, arguing that S'090 used a frequency that was incompatible with the Cobos circuits. *Id.* at *30.

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[19] *Murata Mfg. Co., Ltd. v. SynQor, Inc.*, No. 2012-012209, 2013 Pat. App. LEXIS 5715 (Aug. 19, 2013).

[20] J.A. Cobos & J. Uceda, *Low Output Voltage DC/DC Conversion*, 1994 IEEE 1676 (1994).

S'090 is not limited to any particular frequency, however. In an attempt to impose a frequency on S'090, *SynQor argued* (contrary to its position in this case[21]) that S'090 incorporated S'539 by reference. (*Id.*). SynQor did this because the Figure 4 embodiment of S'539 contains a discussion of the Casey article (A61, col. 4, ll. 44-49), and the Casey article contains a discussion of frequency. So SynQor argued a double incorporation-by-reference (Casey → S'539 → S'090). (*Id.*). SynQor further argued that a person of ordinary skill would have understood Casey's frequencies to reach through *two* incorporations-by-reference, to thereby limit S'090. *Murata,* 2013 Pat. App. LEXIS 5715 at *30. The PTAB explained this argument as follows:

> "Patent Owner also argues, relying on the Casey article, that a frequency incompatibility exists between Steigerwald '090 and Cobos. PO App. Br., 49. Patent Owner represents that the Casey article explains that the Steigerwald '090 isolation stage operates at a switching frequency in the range of 3-10 MHz. *See* Casey article,[13] Steigerwald '090, 3:23-29."
>
> *Id.* at *30.

[21] *See, e.g.,* A878.

The PTAB accepted this argument, *see id.* at *30-*34, in the process finding that "Steigerwald '090 incorporated Steigerwald '539, which further incorporated Casey, *et al.*" *Id.* at *30, n.13.

Thus, at SynQor's urging, the PTAB in the *Murata* case held that Casey modified Fig. 4 of the S'539, which in turn modified S'090's lone embodiment. Here, however (and again at SynQor's urging[22]), the PTAB found that Fig. 4 of S'539 was a "discrete embodiment" of S'539, *unrelated to* the lone embodiment of S'090. (A9). These two conclusions cannot be reconciled. Indeed, SynQor should be judicially estopped from taking a position inconsistent with its winning argument in a prior administrative proceeding on the same patent. *See Trs. in Bankr. of N. Am. Rubber Thread Co. v. United States*, 593 F.3d 1346, 1354 (Fed. Cir. 2010).

Because of the very clear relationship between the "alternative embodiment" of S'539 and the sole embodiment of S'090, the PTAB's reversal of the Examiner should itself be reversed.

[22] *See, e.g.,* A882.

2). The PTAB erred by finding that claims 24-26 were not obvious over S'090 and S'539.

a). The PTAB confused "switching regulators" with "synchronous rectifiers".

The PTAB further erred by finding that claims 24-26 of the '190 patent were not obvious over S'090 and S'539. Claims 24-26 add only voltage levels used at various points in the DC-DC converters. (A10). The PTAB found that the particular voltage levels were common in the prior art (A11), but found that it would not have been obvious to reach claims 24-26 using the system of S'090/S'539. (A11). The PTAB's reasoning was, respectfully, erroneous as a matter of law and unsupported by substantial evidence.

The PTAB's first reason for finding non-obviousness involved what Vicor will refer to as SynQor's "**inductor argument**". The PTAB's take on the inductor argument is best summarized in the following passage from its decision:

> "It is apparent from the above that **avoidance of induction in the current path** was critical to success in Steigerwald '090. **Switching regulators would add inductance**. We therefore disagree that one of ordinary skill in the art would do which is almost expressly excluded from the Steigerwald '090 reference, even though

> an alternative embodiment in Steigerwald '539 might seem to **suggest a substitution in another location**."

(A13) (emphasis added). Here, PTAB has made a fundamental factual error. The error involves confusing "*synchronous rectifiers*" with "*switching regulators*" (*see* quote above). Synchronous rectifiers (*i.e.* controlled rectifiers) are used to rectify (change from AC to DC) current leaving transformers T1 and T2 in S'090. (A61, col. 4, ll. 58-60 and col. 3, ll. 21-28; A4366-A4367). "Switching regulators", on the other hand, are used to regulate to a specific voltage level at the output of a DC-DC converter. (A37, col. 4, ll. 23-28). The difference between "regulation" and "rectification" was explained above in § 0.

Switching regulators have nothing to do with the claims at issue here (claims 20 and 24-26). Claim 20 recites *regulators* in general, but leave open the *type of regulator* (whether "switching" or otherwise). Furthermore, the PTAB found that S'090 teaches regulators generally.[23] (A11, bottom). Thus, under this rejection, it is simply irrelevant whether it would have been obvious to use switching regulators as opposed to other kinds of regulators.

[23] The PTAB found that S'090 teaches "linear regulators", which meet the language of claim 20. A0011.

Switching regulators *are* relevant in claims *not at issue* in this rejection, namely claims 2-4 and 34-38. Those claims contain express requirements for "switching regulators". And it is with respect to those claims that SynQor made its "inductor argument". (A875; A887-A888).

In discussing *claims 24-26* over S'090/S'539, however, SynQor made no "inductor argument". (A945, A948-A949). This is presumably because the synchronous rectifiers of S'539 are simply transistors, with no inductor. (A1183-A1184, ¶6; A56).[24] Thus, in arguing claims 24-26, SynQor instead focused on the incorporation by reference of S'539 into S'090. (A945, A948-A949).

Nevertheless, the PTAB erroneously adopted a SynQor inductor argument directed at other claims, perhaps misled by the linguistic similarity between the terms "switching regulator" and "synchronous rectifier". (A11).

The PTAB's confusion is evident from four sources. First, as noted above, SynQor did not make the "inductor argument" with respect to claims that do not contain "switching regulators". (*Id.*) Second, the

[24] Even if SynQor were right about its alleged prohibition on inductors in the output path in S'090, S'090 actually uses transistors in the output path as regulators, Fig. 1, numerals 50, 51, 60, and 61).

synchronous rectifiers of S'539 have no inductor, and thus would not be subject to the inductor argument in any case.[25] (A1183-A1184, ¶6; A56). Third, the PTAB's discussion of "substitution" of switching regulators into S'090 (A13) makes no sense for claims that do not recite switching regulators. Fourth, the PTAB actually uses both terms ("synchronous rectifiers" and "switching regulators") seemingly interchangeably on page A13. For these reasons, it is evident that the PTAB's finding was not supported by substantial evidence.

b). The declaration of SynQor's CEO is legally irrelevant and does not amount to substantial evidence.

The PTAB next relied on the declaration of Dr. Schlecht (named inventor and CEO of SynQor) for the proposition that substituting synchronous rectifiers into S'090 "could lose efficiency". (A12-A13).

First, Dr. Schlecht's declaration is legally irrelevant. For the reasons provided in § Argument.B.1., above, the unified S'090/S'539 reference *expressly teaches* the use of synchronous rectifiers *in a single document*. There is no need to find than any substitution is "obvious".

[25] In fact, synchronous rectifiers are embodied in both S'539 and the '190 patent as MOSFET transistors. (A1183-A1184, ¶6; A56; A38, col. 6, ll. 22-31).

Second, even if the PTAB were correct that S'539's "alternative embodiments" statement did not modify S'090 sufficiently to anticipate, the incorporation-by-reference and the similarities between S'090's lone embodiment and Fig. 4 of S'539 represent an extremely strong motivation to combine, against which the declaration of an interested party is not substantial evidence.

Third, Dr. Schlecht's declaration is legally irrelevant in terms of efficiency, because it states only that the efficiency of synchronous rectifiers would be *approximately equal* to that of diode rectifiers. (A1193, ¶30). To the extent that synchronous rectifiers and diodes are known alternatives for the same function having similar performance, their substitution is obvious. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417 (2007) ("a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.").

Fourth, Dr. Schlecht's argument concerning potential disincentives to use synchronous rectification contradicts his own prior statements to a court on the subject. Specifically, *Dr. Schlecht's* 1998 technology tutorial (A4344-A4378), presented to a district court, makes

the case that synchronous rectification had been obvious since at least the early 1990s. (A4367). In *Dr. Schlecht's own words*:

> "**Synchronous rectification**, i.e. using a MOSFET in place of a diode, **is not a new idea**. It has been discussed and used in the power electronic community for at least 15-20 years. However, in the early years it was not economical to use synchronous rectifiers. **More recently (starting in the early 1990's)** the MOSFETs we have available are much better than those before this time….As a result, **synchronous rectification has recently become more prevalent, although it was well understood and anticipated for nearly two decades**."

(A4367) (emphasis added). Dr. Schlecht's personal financial interest in the outcome of the case (A18), combined with his prior admission concerning the obviousness of synchronous rectification, reveal his current declaration to be a litigation-driven fiction. It has no probative value as a matter of law. *See analogously Del. Valley Floral Grp., Inc. v. Shaw Rose Nets, LLC*, 597 F.3d 1374, 1381-1382 (Fed. Cir. 2010) (in the context of summary judgment, a party cannot create an issue of fact with contradictory testimony); *NLRB v. Elias Bros. Big Boy, Inc.*, 327 F.2d 421, 426-27 (6th Cir. 1964) (NLRB's decision did not

have substantial evidence support because the Board credited the testimony of an interested witness over other evidence).

c). The PTAB erred in its analysis of secondary considerations

The PTAB lastly erred by holding that SynQor provided evidence of commercial success that "would have been sufficient to overcome the Examiner's conclusion of obviousness". (A18). The PTAB erred in two ways. First, the PTAB lacked substantial evidence to conclude that there was commercial success. Second, the PTAB adopted a formulaic approach to commercial success, causing it to overlook strong, objective evidence of obviousness.

i). The PTAB's finding of commercial success is not supported by substantial evidence.

First, the conclusion of commercial success is unsupported by substantial evidence. The PTAB relies heavily on a jury verdict of infringement in the *Artesyn* litigation—a case to which Vicor was not a party. (A15-A16). The PTAB's first error in this regard is that claims 24-26 were not asserted at the *Artesyn* trial—the jury rendered no verdict on these claims. (A4436-A4497). Thus, the trial evidence could not have informed the PTAB about the commercial success or failure claims 24-26.

See MeadWestVaco Corp. v. Rexam Beauty & Closures, Inc., 731 F.3d 1258, 1264-65 (Fed. Cir. 2013) (secondary considerations must be analyzed on a claim-by-claim basis).

The PTAB attempted to patch this hole in its logic by referring to a data sheet for a Bel-Fuse product (07CM-20S30S). (A16). The Bel-Fuse data sheet, according to the PTAB, described "output voltages of 8 and 12 volts from a 48 volt input." (*Id.*). According to the PTAB, this demonstrated the inclusion of claims 24 and 25 in the commercial success evidence. (*Id.*).

There are numerous errors with this reasoning. First, the PTAB still lacks evidence to support its decision as to claim 26. (A16). Second, the Bel-Fuse product shown in the data sheet was not accused of infringement at trial, and the East Texas jury rendered no verdict on it. (A4436-A4497). And standing on its own, the data sheet provides no evidence that the products would fall within the scope of any claims of the '190 patent. (A3647-A3648). For example, there is no evidence of controlled rectifiers and the waveform requirements,[26] nor any evidence

[26] *E.g.* in claim 20 "each controlled rectifier being turned ON and OFF in synchronization with the voltage waveform across a primary winding to provide an output".

of many of the dependent claims. Furthermore, there is nothing tying Bel-Fuse products in the chosen data sheet to any actual sales.

The PTAB's decision further provided no substantial evidence of nexus. In fact, the decision has no explanation of why it found a nexus to exist. The decision does state that:

> "We are informed that millions of infringing units were sold, and that the end products are commensurate in scope with the instant claims. PO Reb. Br. at 22-23 and 26-28. We are also informed that there is no substantially non-infringing use for the system, and conversely that there are no non-infringing alternatives, resulting in $80 million in lost profits to SynQor. *Id.* at 25. See also the Schlecht Declaration, A1, paras 59-63."

(A15-A16). The PTAB's fact findings here lack substantial evidence. The PTAB's first finding cites no evidence other than SynQor's rebuttal brief below, at pages 22-23 and 26-28. The brief, however, has no such pages, as it is only 15 pages long. (A1030 and A1046). The citation to Dr. Schlecht's declaration at ¶¶59-63 recounts only Dr. Schlecht's recall of SynQor's consultant's trial testimony, and is limited to the claims asserted at trial (not claims 24-26). (A1200, ¶60). Furthermore, the PTAB's reliance on SynQor's assurances that there

were no substantial non-infringing alternatives *for every claim* would be odd, given that claims 24-26 relate to voltage levels. One could simply change voltage levels to fall outside the scope of the claims. For example, the PTAB found that the Bel-Fuse product (07CM-20S30S) could output 8V ***or*** 12V (A16). Yet the PTAB still accepted SynQor's assurance that there were no non-infringing alternatives for claim 25, which is limited to 12V. Likewise, other claims in the '190 patent appear to be mutually exclusive (claims 17 and 18, *e.g.*), meaning that if one is infringed, the other cannot be.

The PTAB's possible conclusion of nexus further lacks substantial evidence because the claims do not recite an intermediate bus, and the intermediate bus is critical to the operation of the "intermediate bus architecture" for which SynQor seeks to claim credit. *See Ormco Corp. v. Align Tech. Inc.*, 463 F.3d 1299, 1312 (Fed. Cir. 2006) (commercial success driven by an unclaimed feature is not probative).

An intermediate bus is an electrical connection over a distance between an isolating front end and downstream POL, as shown in Figure 2 from the White article (reproduced above on page 18). (A3416). In a 2004 article, Dr. Schlecht himself (named inventor and SynQor

CEO) admitted that without separation over a distance between the bus converter and downstream POLs, there was *no incentive* to use an intermediate bus architecture. (A3451-3453). In his article, Dr. Schlecht describes an engineering team comparing DPA and IBA for a particular application. (A3451). Ultimately, the team chose DPA, because the configuration of the board would have forfeited any advantage of IBA. (A3452, left column). Specifically, the advantage was forfeited by placing the bus converter too close to the POLs. In Dr. Schlecht's own words:

> "The engineers then discussed the advantage offered by the IBA approach in that it allowed the power to be distributed around the load board at a relatively high voltage (12V) and a correspondingly small current.....In the end, if they decided to go forward with the IBA approach, the engineers knew they would have to keep the POL converters near the bus converter, and therefore not be able to take advantage of a higher distribution voltage."

(A3452). There can be little dispute that the claims do not recite a bus separating the bus converter from the POLs over a distance. Beyond the claim language, Dr. Schlecht provides key evidence on this point, which could not be clearer. In his declaration, he states:

> "The '190 patent does not specify the physical length of the bus, and the patent claims are not limited to any specific length bus".

(A1198, ¶54). The claims likely lack this key component of IBA because the '190 patent never disclosed it.

The PTAB ignored the substance of the admissions by Dr. Schlecht, instead focusing on a straw man argument. The chosen straw man was the use of the *literal* term "intermediate bus architecture" in the claims. (A18). Not surprisingly, the PTAB was able to knock this straw man down, holding that "[t]he fact that claims 1 and 20 do not recite the particular set of words 'intermediate bus architecture' does not persuade us of a lack of nexus." (A17).

The PTAB's reasoning, however, misses the import of SynQor's admissions entirely. The import is that the '190 patent fails to claim *any structure* (whatever it may be called) that would connect the bus converter over a distance to the POLs as separate devices, and thereby preserve a benefit from using IBA. (A1199, ¶54). Under these circumstances, even if claims 24-26 were commercially successful, that success is not attributable to any contribution of Dr. Schlecht to the art.

For these reasons, the PTAB's finding of commercial success was not supported by substantial evidence.

ii). The PTAB erred in its overall approach to evaluating secondary considerations.

Relying on the dubious chain of reasoning founded on events in an East Texas jury room (in a proceeding to which Vicor was not a party), the PTAB mentally checked off "infringement" and (possibly) "nexus" boxes. This led the PTAB—seemingly inevitably—to a finding of non-obviousness. (A18). Such a formulaic approach to secondary considerations (*infringement + nexus (?) = non-obviousness*), however, was legal error. *See, e.g. KSR*, 550 U.S. at 415 ("We begin by rejecting the rigid approach of the Court of Appeals."). In the present case, there was strong evidence indicating that no inference of non-obviousness should be drawn, and the PTAB erred by failing to consider this evidence.

There is no dispute that "secondary considerations" can be relevant to the question of obviousness. *See id.* Although secondary considerations are often invoked to rebut a case for obviousness, it is also clear that secondary considerations can make a case for *invalidity* stronger. *See Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)("Such

secondary considerations as commercial success…might be utilized…. As indicia of **obviousness or nonobviousness**, these inquiries may have relevancy.") (emphasis added).

The "commercial success" of a product embodying a patent claim *can be* relevant to the obviousness of that claim. *See id.* This is because it is reasonable to assume that industry participants want to make money as soon as possible. If they instead delay until shortly after an inventor discloses the claim, one could infer that the only obstacle to making money with the invention was the non-obviousness of the claim. This inference is the foundation upon which the relevance of "commercial success" evidence rests. *See In re Fielder*, 471 F.2d 640, 644 (C.C.P.A. 1973).

The inference, however, is only that. It can be weakened, or even reversed, by other evidence in the case. *See Merck & Co. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1376-77 (Fed. Cir. 2005). As Learned Hand explained in *Ruben Condenser v. Aerovox*:[27]

> "While it is always the safest course to test a putative invention by what went before and what came after, it is

[27] *Ruben Condenser Co. v. Aerovox Corp.*, 77 F.2d 266 (2d Cir. N.Y. 1935).

> easy to be misled. Nothing is less reliable than uncritically to accept its welcome by the art, even though it displace what went before. If the machine or composition appears shortly after some obstacle to its creation, technical or economic, has been removed, we should scrutinize its success jealously**....**"

Ruben Condenser Co. v. Aerovox Corp., 77 F.2d 266, 268 (2d Cir. 1935).

Had the PTAB moved beyond its dubious findings of infringement and nexus, it would have faced a question very difficult to answer in SynQor's favor, namely "is the commercial success actually persuasive?" This is the question the PTAB needed to address, but did not. When fully considered, the evidence demonstrates the *obviousness* of the claims of the '190 patent.

The present case represents one of the stranger allegations of "commercial success" that the undersigned has ever encountered. In a normal case, the patent owner alleges that the *patent's disclosur*e communicates an improvement to the industry, and the industry then adopts the improvement. In this case, however, SynQor does not allege that the disclosure of the '190 patent communicated the claimed

invention to anyone. In fact, SynQor believes the opposite is true—that the '190 patent's disclosure was insufficient to convey the claims even to highly skilled artisans. For example, SynQor argued below that:

> "experienced engineers were amazed by SynQor's technology (Ex. 49, PTX 135 at 1-2), and **had difficulty implementing it even with access to SynQor's** products/datasheet/**patent**."

(A583) (emphasis added). The method by which the industry learns of a claimed technology is important, because it affects the strength of the "commercial success" inference. If there is no event that provided a new insight to the industry, then it is very difficult to infer a change in the industry's behavior based on the introduction of a non-obvious invention. Instead, the more likely inference becomes that the industry started using *available* technology when it became *economically worthwhile* to do so.

It is easy to see why SynQor argues that the '190 patent did not communicate its alleged invention: the specification of the '190 patent has very little to do with the claims that ultimately issued. (*See* § 0). Instead, the '190 patent's technical disclosure is almost entirely directed to single-housing DPA "brick" converters used in the very same prior

art that SynQor criticizes. (*Id.*). The figures of the '190 patent have only a single output, and even reverse the order of "isolation followed by regulation" that SynQor later inserted into the claims. (A29-A35). For example, Fig. 1 is shown below:

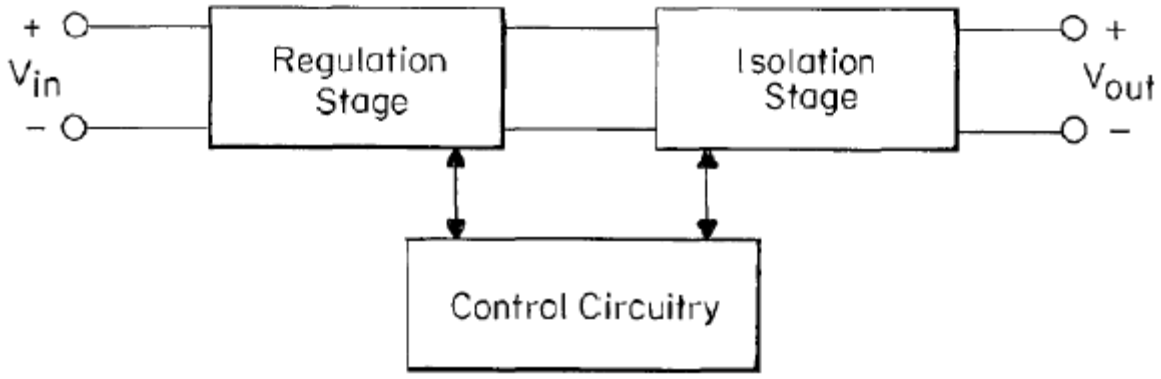

FIG. 1

(A29). SynQor's only basis for written description support is found near the end of the specification (col. 14). There, a patent-lawyeresque statement proposes two different modifications, one to swap the order of regulation and isolation, and the other to provide multiple outputs. (A42, col. 14, ll. 31-39). If one applies these modifications to one of the main embodiments, one can then have a highly technical debate about written description support for the claims. Regardless of how that debate may turn out, however, it is apparent that the '190 patent specification is not a document that would *convince* the industry of the

benefits of an intermediate bus architecture. No benefits to such an architecture are described. Furthermore, no guidance is given that the principal embodiments are inferior, and that superior results could be obtained by performing the modifications in column 14.

Presumably for these reasons, SynQor did not take the position that its patent disclosure communicated anything to the industry. Rather, SynQor alleged (citing Dr. Schlecht's testimony at A1189-A1190) that its employees conducted a series of unrecorded personal meetings with industry members. During these meetings, SynQor employees allegedly convinced the industry that a concept called "Intermediate Bus Architecture", would revolutionize power conversion technology and sweep aside the prior art. For example, Dr. Schlecht testified below that:

> "**I believed that the technology I invented**, and was actively developing, **would revolutionize the power converter industry**….Having established business relationships with its customers, **SynQor introduced the concepts of the Unregulated and Semi-Regulated Intermediate Bus Architectures ("IBA") to the Hewlett-Packard Company and Cisco**

> **Systems, Inc. at least as early as the winter of 2000/2001**."

(A1189-A1190, ¶¶4 and 6) (emphasis added). Likewise, SynQor's attorneys argued that:

> "The increasingly **unsuitable DPA 'bricks' that dominated the switch market (A36 at 22; A39 at 1) were swept aside by Dr. Schlecht's design**, which Cisco and others widely adopted **after Dr. Schlecht demonstrated its value**."

(A905) (emphasis added). SynQor alleges that it developed a revolutionary new technology, and demonstrated the superiority of that technology in meetings held in the winter of 2000/2001. The problem with SynQor's allegations is that they are inconsistent with the contemporaneous documentation. The '190 patent disclosure, for example, certainly does not reflect SynQor's awareness of a revolutionary new technology. Had SynQor believed that IBA was as revolutionary as it now claims, surely IBA would be described in the principal embodiments of the patent specification, and not just be *allegedly derivable* through the application of multiple statements of

alternative. The '190 patent could also reasonably have been expected to discuss the advantages of IBA—but it does not.

Nor do SynQor's own documents reflect SynQor's version of events. A telling December, 2000 email (*i.e.* during the time SynQor says it was convincing others of the superiority of IBA) from a SynQor employee (Dirk Johnson) describes a conversation with Bob Marshall of Cisco. (A3160). As SynQor's employee noted, Cisco rejected SynQor's DPA "brick" converters. The email states:

> "Bob is evaluating different platforms for his next generation DSL card….**He does not feel that he can economically accommodate this requirement with isolated DC/DC converters**."

(*Id.*) (emphasis added). SynQor's employee next reports that *Cisco suggests* an Intermediate Bus Architecture:

> "He would like to **convert to a single voltage and use discretes**[28] **to accomplish the rest**."

(*Id.*) (emphasis added). SynQor's employee then apparently attempted to sell one of SynQor's DPA-related "brick" products, the

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[28] Here, the term "discretes" refers to POL converters that have been assembled from available components, rather than sold as modules. (A4393).

Tera 12V unit (A3212). Cisco, however, rejected it. SynQor's employee states:

> "We looked at the **Tera 12V unit**. We could not get enough power at 85C with only 150LFM. He also feels like that solution is expensive."

(*Id.*) (emphasis added). Then, SynQor's employee mentions that Cisco is interested in a bus converter. SynQor's employee asks, "**Is this a product that we plan to offer?**" (*Id.*) (emphasis added). This document shows that SynQor was learning about IBA from the industry—not the other way around.

In fact, SynQor did not offer an IBA-related product (its "BusQor" converter) until 2002 (A4309), *five years after* SynQor's original patent filing leading to the '190 patent. It is unreasonable to think that SynQor, having invented a technology in 1997 that it believed to be "revolutionary", would wait so long to offer its revolutionary new product. It is further unreasonable to conclude that SynQor's salespeople in 2000 would de-emphasize products *they actually had to sell*, in order to promote products *they did not know would be offered*. SynQor's internal email quoted above confirms this point. (A3160).

The most plausible explanation of SynQor's behavior is that SynQor did not understand IBA to be important. A December 2002 SynQor product roadmap confirms this. (A3210-A3267). The roadmap spends the first 27 pages focusing on SynQor's DPA "brick" products, before even mentioning an Intermediate Bus Architecture product. (A3210-A3236). Slide 32 provides SynQor's discussion of "when a bus converter makes sense". (A3241). Given that SynQor had allegedly convinced the industry of the revolutionary nature of IBA two years earlier, one might expect the answer to have been "always!" Yet SynQor's internal discussion is much more muted, recommending IBA only where "the costs of designing and implementing POL nonisolated converters are less than standard brick solution." (A3241).

Perhaps the most telling document, however, is Dr. Schlecht's *2004* article entitled "Choosing an On-Board Power Architecture". (A3451-A3453). This article was published seven years *after* SynQor's patent application was filed, and four years *after* SynQor allegedly convinced the industry of the superiority of IBA over DPA. The article begins with the question "**Intermediate Bus Architecture (IBA) or Distributed Power Architecture (DPA) which one do you**

choose?" (A3451) (emphasis added). Because this article was published in 2004—four years *after* SynQor allegedly convinced the industry of the superiority of IBA—there should be no doubt about the answer to this question. Dr. Schlecht should wholeheartedly endorse IBA as the clear winner. Instead, his answer was as follows:

> "It would be nice if one approach were so much better than the other that you could answer this question definitively for all scenarios. But that is not the case. Instead, often the two approaches are quite close to each other in performance, and even the definition of 'better' is at best complex."

(A3451). These are not the words of a person who led an IBA revolution that "swept aside" the prior art. (A905). Instead, they are the words of a person who is coming to grips with a technology whose value is unclear to him (seven years after his patent application was filed).

The parties do agree that the use of IBA became more prevalent in the 2002-2005 timeframe (five to eight years after SynQor's first patent application). This was not due to SynQor's introduction of the

technology, however, but rather due to the decreasing cost of IBA-related components.

Vicor provided compelling, objective evidence that the availability of inexpensive POL converters was responsible for the increased use of IBA in this timeframe. (A760-A762). The relationship between POL cost and the desirability of IBA was noted in SynQor's internal presentation discussed above, which recommended using IBA where "the costs of designing and implementing POL nonisolated converters are less than standard brick solution." (A3241). This was further confirmed by third-party publications, such as that from White (2003). White explained that:

> "The name Intermediate Bus Architecture most often means a two level distributed power system like that illustrated in Figure 2. The second level of distribution is called the Intermediate Bus. This use of this architecture has increased greatly in the last two years [6]. **The drivers for the wide adoption of the Intermediate Bus Architecture are**:
>
> • The large number of supply voltages needed in systems and on individual circuit cards in today's systems and

> • **The rapidly decreasing cost of nonisolated, point-of-load (POL) dc-dc converters**."

(A3416) (emphasis added). Notably, White does not say that IBA came about when SynQor introduced it.[29] Rather, White states that the driving factors for the adoption of IBA were increasing numbers of supply voltages needed and the decreasing cost of POLs to supply those voltages. (A3416).[30] SynQor does not contend to have had anything to do with improving POL converters. As noted in *Ruben*,

> "[i]f the machine or composition appears shortly after some obstacle to its creation, technical or economic, has been removed, we should scrutinize its success jealously…."

Ruben Condenser Co. v. Aerovox Corp., 77 F.2d 266, 268 (2d Cir. 1935) (Judge Hand).

It was likely the expansion in the use of IBA in the 2002-2005 timeframe that finally led SynQor to see its value. In June of 2005, SynQor went back to the patent office and canceled its original claims

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[29] In fact, White credits one of his competitors, Brian Narveson, for the creation of IBA in 1996. (A3416).

[30] *See also* A1549, a 2003 DATEL Application Note ("The concept [IBA] is not new; however, it is rapidly becoming affordable—compellingly so—as more vendors announce related products"); and A4392-4393.

directed to its main embodiments. Then, eight years after its first patent application was filed, SynQor introduced its very first claims directed to a system having an isolating, non-regulating stage feeding multiple regulating, non-isolating outputs.[31] The application issued as the '190 patent in 2006, and SynQor filed suit on the '190 patent in 2007.[32]

With this context, SynQor's allegation of "commercial success" must be seen in a very different light. Because SynQor did not communicate the technology it claims to the industry, no inference can be drawn about the industry's inability to conceive of the technology prior to such a communication. Likewise, the fact that that certain industry participants adopted the technology when its components became cost-effective shows that the technology was available all along—just not particularly economical. Furthermore, any inference that could be drawn from a jury's finding of infringement looks very different when one understands that SynQor first drafted the relevant claims years after the technology had become more popular.

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[31] *See* U.S. App. Ser. No. 10/812,314, Amendment of June 13, 2005.

[32] *SynQor, Inc. v. Artesyn Techs., Inc.*, *et al.*, Case No. 2-07-cv-00497 (E.D. Tex.), filed Nov. 13, 2007.

Had the PTAB properly considered this evidence, it would have found differently. Instead, however, the PTAB shut down as soon as it had reasoned its way to infringement and (possibly) nexus. (A17-A18). While the PTAB *mentions* Vicor's POL evidence (but not other evidence), the PTAB's decision does not say whether this evidence was persuasive. (*Id.*). Instead, the PTAB writes its decision as if Vicor's evidence were legally superseded by a finding of infringement and nexus. (A18). This applied the law of secondary considerations formulaically, contrary to Supreme Court precedent. *KSR*, 550 U.S. at 415. The PTAB thus erred as a matter of law by failing to consider whether any properly-founded commercial success was *actually persuasive* and by failing to consider evidence relevant to that question.

3). The PTAB erred by failing to affirm the Examiner's rejection of claims 1-19, 24, 28 and 31 over the Cobos-based references.

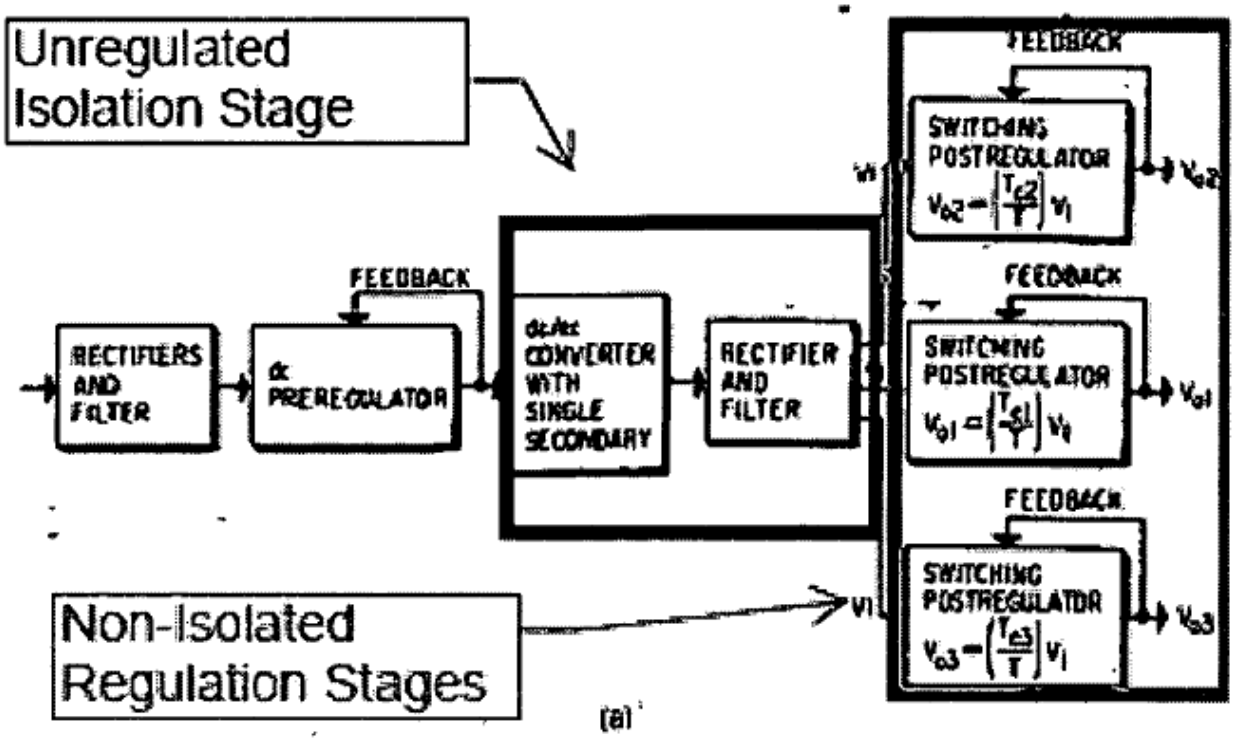
The PTAB further erred by reversing the Examiner's determination that claims 1, 5-19, 24, 28, and 31 under 35 U.S.C. § 103(a) as being unpatentable over S'090/S'539 and Cobos and claims 2-4 as further obvious over S'090/S'539, Cobos and Pressman. The PTAB reversed these rejections because Cobos purportedly "does not rectify

the deficiencies of the underlying Steigerwald references". (A19). As discussed above (§§ Argument.B.1. and Argument.B.2.), however, the PTAB erred by finding deficiencies in S'090/S'539. The PTAB's reasoning here is thus erroneous for the same reasons and its decisions should be reversed.

4). The PTAB erred by failing to affirm the Examiner's rejections of claims 1-38 over Cobos in view of Pressman.

The PTAB further erred by reversing the Examiner's rejections of claims 1-38 over Cobos in view of Pressman.

Pressman in Fig. 3-4(b) teaches a multi-stage power system, where an unregulated isolation stage feeds multiple non-isolating regulators. This is shown in the figure from Pressman below, where Vicor labeled the isolating stage and the multiple downstream regulators (A519):



Pressman states that this architecture can be used to "generate a multiplicity of different output voltages at high efficiency". (A171-A172). Pressman does not disclose the internal details of the unregulated isolation stage, and thus it is unknown from Pressman alone whether controlled rectifiers are used. Cobos, however, provides an isolating, non-regulating stage that meets the related elements of the claims. This much does not appear to be disputed. (A20-A22).

The PTAB had three bases for reversing the Examiner's rejection over Cobos and Pressman. (*Id.*). First, the PTAB found that Pressman's Fig. 3-4(B) uses switching regulators (which have high efficiency), not series-pass post-regulators, "which would result in low

efficiency". (A22). Second, the PTAB held that the proposed combination might be less efficient than using Cobos alone. (A21-A22). Third, the PTAB found "commercial success". (A22). Each of these findings is either erroneous in its application of the law or unsupported by substantial evidence (or both).

The PTAB's first reason was expressed as follows:

> "We also find merit to the Patent Owner's contention that Pressman's description of Figures 3-4(B) discusses that multiple output voltages may be obtained at high efficiency by using multiple switching post-regulators (one for each output) rather than series-pass post-regulators (which would result in low efficiency). We then are left principally with hindsight as the possible motivation for making this combination."

(A22). The PTAB's conclusion of hindsight is not supported by substantial evidence. It is noteworthy that the PTAB, Vicor and the Examiner *are in agreement* as to the relevant teachings of Pressman. For example, Vicor agrees with the PTAB that Pressman teaches a plurality of switching postregulators at the output. The regulators are visible on the right-hand side of Figure 3-4(B) (shown above), and the PTAB's finding on this point is thus well-supported. (A171). Vicor

further agrees with the PTAB that, by using these switching regulators, "multiple output voltages may be obtained at high efficiency". (A172). Pressman says exactly this on page 83. (*Id.*). Vicor also agrees with the PTAB that "Pressman does not teach using series-pass regulators (which would result in lower efficiency)." (A171-A172).

These findings, however, are precisely the motivation to combine put forward by Vicor (A519) and adopted by the Examiner. On page 54 of the request for *inter partes* reexamination (A519), for example, Vicor quoted Pressman page 83, and stated that:

> "Pressman thus motivates the addition of the claimed regulation stages to Cobos to provide 'a multiplicity of different output voltages at high efficiency,' rendering claim 1 obvious."

(A519). The Examiner adopted this reasoning in his Right of Appeal Notice. (A850). Having found exactly the same facts (and no others), the PTAB's conclusion that the combination is based primarily on hindsight is inexplicable, and certainly not based on substantial evidence.

The PTAB's second finding—that the combination might actually be less efficient than using Cobos alone and is therefore non-obvious—is

erroneous as a matter of law. Even if one disregards the PTAB's finding that Pressman teaches the use of switching postregulators to achieve high efficiency, and even if one then assumes that the use of Cobos' converter in Pressman's architecture would be less efficient, this does not remove an obvious combination from the public domain. A well-known solution does not become subject to re-patenting once a better solution comes along. Computers using vacuum tubes did not become patentable when computers using transistors came into being, any more than chemotherapy is now a *patentable* treatment for cancer where better gene therapies are available. *See, e.g., In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004) ("our case law does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention."). Likewise here, even if we accept that Cobos' Fig. 14a provides a more efficient method of generating multiple outputs, it does not remove Pressman's older, but still known method from the prior art.

Furthermore, even if one ignores the PTAB's confirmation of Pressman's express motivation, Cobos teaches a known converter that

can be used in for its known function in Pressman's known system to provide the desirable goal of multiple outputs, without any surprising results. (A727). The combination is thus obvious, even if other solutions might be more efficient. *See KSR*, 550 U.S. at 427-28.

The PTAB's third reason involved the same commercial success findings discussed above in §§ Argument.B.2).c).i). and Argument.B.2).c).ii). With respect to claims not asserted in the *Artesyn* litigation, the discussion of the PTAB's errors applies in the same way. In particular, the PTAB made no attempt at a claim-by-claim finding of commercial success for this rejection of claims 1-38.

With respect to all claims, the arguments in § Argument.B.2).c).ii). apply equally here. The PTAB should have considered all relevant facts and examined the persuasiveness of the commercial success inference, rather than mechanically applying the formula *infringement + nexus (?) = non-obviousness*.

For these reasons, the PTAB's decision to reverse the Examiner's rejection of claims 1-38 as obvious over Cobos in view of Pressman should be vacated and remanded.

CONCLUSION

Vicor respectfully requests that this Court reverse the PTAB's decision to reverse the Examiner with respect to the anticipation of claims 20-23, 27, 29, 30, 32 and 33 over S'090/S'539, and with respect to the obviousness of claims 1-19, 24, 28 and 31 over S'090/S'539 in view of Cobos and/or Pressman. Vicor further respectfully requests that the PTAB's decisions with respect to obviousness of claims 24-26 over S'090/S'539 and claims 1-38 over Cobos in view of Pressman be vacated and remanded for further consideration by the PTAB.

Date: September 2, 2014

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ADDENDUM

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VICOR CORPORATION
Requester

v.

SYNQOR, Inc.
Patent Owner and Appellant

Appeal 2014-001733
Reexamination Control 95/001,702[1]
Patent No. US 7,072,190 B2[2]
Technology Center 3900

Before JAMES T. MOORE, STEPHEN C. SIU, and
DENISE M. POTHIER, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Patent Owner SynQor appeals under 35 U.S.C. §§ 134(b) and 315(a) (2002) from the rejection of claims 1-38 as set forth in the Right of Appeal Notice ("RAN") mailed November 26, 2012. Requester Vicor Corporation

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[1] Filed by Vicor Corporation on September 8, 2011.
[2] Issued July 4, 2006 to Martin Schlecht and assigned to SynQor, Inc. (the "'190 patent"). The '190 patent issued from Application 10/812,314, filed March 29, 2004.

filed a Respondent Brief on March 26, 2013. The Examiner mailed an Examiner's Answer on June 11, 2013, which incorporated the RAN by reference. The Patent Owner filed a Rebuttal Brief on July 11, 2013. Oral argument was conducted before a panel of this Board on March 19, 2014 in combined Reexamination Proceeding Appeals 2014-001167 and 2014- 001173 and a transcript of the proceedings will be made of record. We have jurisdiction under 35 U.S.C. §§ 134 and 315.

We REVERSE.

Much litigation has occurred concerning this and related patents. The Patent Owner observes that the Federal Circuit "upheld the District Court's decision finding validity of all challenged claims of U.S. Patent 7,072,190."[3] Invalidity in an infringement action can be an affirmative defense raised by a defendant. The District Court can find claims "not invalid" on those grounds raised, but the issue presently faced upon the reexamination proceeding appeal is different; more specifically, whether the challenged claims are patentable. To the extent the evidence relied upon during litigation and decisions of the District Courts and Federal Circuit are informative or persuasive, we have considered them as such.

At this stage, the Examiner has concluded that the claims are not patentable, and it lies with the Appellant Patent Owner to argue persuasively otherwise.

The '190 Patent concerns power conversion. The claims generally describe a two-stage direct current to direct current power conversion system that has two separate stages – one for isolation and one for the actual voltage

[3] Patent Owner Rebuttal Brief 1, hereinafter "PO Reb. Br. 1"

conversions needed. The combination of these separate stages is said to provide improved efficiency, size, and cost. PO App. Br. 2.

Claim 1 is representative, and reproduced below, with paragraphing added for sake of clarity.

1. A power converter system comprising:

a DC power source;

a non-regulating isolation stage comprising:

a primary transformer winding circuit having at least one primary winding connected to the source; and

a secondary transformer winding circuit having at least one secondary winding coupled to the at least one primary winding and having plural controlled rectifiers, each having a parallel uncontrolled rectifier and each connected to a secondary winding, each controlled rectifier being turned on and off in synchronization with the voltage waveform across a primary winding to provide an output,

each primary winding having a voltage waveform with a fixed duty cycle and transition times which are short relative to the on-state and off-state times of the controlled rectifiers; and

a plurality of non-isolating regulation stages, each receiving the output of the isolation stage and regulating a regulation stage output while the fixed duty cycle of the isolation stage is maintained.

EVIDENCE OF RECORD

The Examiner relies upon the following prior art in rejecting the claims on appeal:

Steigerwald	US 5,274,539	December 28, 1993
Steigerwald	US 5,377,090	December 27, 1994

J.A. Cobos & J. Uceda, "*Low Output Voltage DC/DC Conversion*" 0-7803-1328-3/94, IEEE (1994).

Abraham I. Pressman, *Switching and Linear Power Supply Power Converter Design*, Hayden Book Company, New Jersey (1977).

THE REJECTIONS

I. Claims 20-23, 27, 29, 30, 32 and 33 stand rejected under 35 U.S.C. §102 (b) as anticipated by Steigerwald '090 and Steigerwald '539.

II. Claims 24-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090.

III. Claims 1, 5-8, 11-13, 17, 18, 24, 28, and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, and Cobos.

IV. Claims 2-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, Cobos, and Pressman.

V. Claims 9, 10, 14-16, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, and Cobos.

VI. Claims 1-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cobos and Pressman.

VII. Claims 34-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cobos and Pressman.

VIII. Claims 35-38 stand rejected under 35 U.S.C. § 103(a) over Steigerwald '090, Steigerwald '539, Admitted Prior Art, and Pressman.

GENERAL ISSUES

Are the cited references properly combinable? The Patent Owner asserts legal issues with the anticipation combination of the two Steigerwald references, and further technical issues, which render the remaining art unsuitable for combination. The Requester asserts the combination is proper by incorporation, and that the technical issues would be easily resolved by one of ordinary skill in the art.

Is the evidence of secondary considerations sufficient to overcome the evidence of obviousness that may exist? The Patent Owner relies heavily on the litigation evidence. The Requester doubts its value.

I. *The Rejection of Claims 20-23, 27, 29, 30, 32 and 33 as anticipated under 35 U.S.C. §102 (b) Steigerwald '090 and Steigerwald '539.*

Claim 20 reads as follows, with paragraphing added for clarity:

20. A power converter system comprising:
a DC power source;
a non-regulating isolation stage comprising:
a primary transformer winding circuit having at least one primary winding connected to the source; and
a secondary transformer winding circuit having at least one secondary winding coupled to the at least one primary winding and having plural controlled rectifiers, each having a parallel

> uncontrolled rectifier and each connected to a secondary winding, each controlled rectifier being turned on and off in synchronization with the voltage waveform across a primary winding to provide an output; and
>
> a plurality of non-isolating regulation stages, each receiving the output of the isolation stage and regulating a regulation stage output.

This rejection was adopted from the Request, pages 8-26. RAN 3.

In short, the Examiner has found that Steigerwald '090 teaches an extension of Steigerwald '539, in which multiple output voltages may be provided. This was found to be accomplished by replacing the single regulation stage 30, which in the '539 Patent is upstream of the isolation stage, with multiple regulation stages that are downstream of the isolation stage. Because each regulation stage may regulate to a different output voltage, the Requester and Examiner conclude that multiple output voltages may be provided using only a single non-regulating isolation stage. Steigerwald '090 2:44-50.

The first question raised is whether this rejection is a proper rejection. The Patent Owner asserts that the combination of Steigerwald '090 and Steigerwald '539 is improper because there is no proper incorporation by reference, and that a composite embodiment created by the combination fails to describe an embodiment, which anticipates the claims. PO Reb. Br. 3.

We first observe that the Steigerwald '090 uses the following language to incorporate the '539 Patent:

> This application is related to commonly assigned U.S. Pat. No. 5,274,539 of R. L. Steigerwald and R. A. Fisher, issued Dec. 28, 1993, and to commonly assigned abandoned U.S. patent application Ser. No. 811,631 of R. L. Steigerwald, filed Dec. 23, 1991, both of which are incorporated by reference herein.

Steigerwald '090 1:6-12.

Inasmuch as the text of the documents can be said to be "incorporated" we will for purposes of discussion presume that this language can be thought of as sufficient to bring the raw text of the parent applications into the continuation-in-part application. However, the incorporation is insufficient to go beyond that, as it does not identify any particular sections or specific subject matter to be associated with particular embodiments of the Steigerwald '090 description.

We disagree with the Requester that Steigerwald '090 is an "extension" of an example in Steigerwald '539. Request 9. The Requester states that the "extension" is accomplished by "replacing" the single regulation stage 30, which in the '539 Patent is upstream of the isolation stage, with multiple regulation stages that are downstream of the isolation stage. Because each regulation stage may regulate to a different output voltage, the Requester urges that multiple output voltages may be provided using only a single non-regulating isolation stage. To this end, the Requester cited Steigerwald '090, 2:44-50.

Steigerwald '090 at column 2:44-50 does not really describe what the Requester states it does. We reproduce the entire paragraph found at Steigerwald '090, 2:41-56 below.

> Output voltages + V1, +V2, . . . are obtained from the positive dc bus voltage via series regulators 50, 51 ... , respectively, to a solid-state phased-array radar T /R module 54. Output voltages –V1, - V2, ... - Vm are obtained from the negative dc bus voltage via series regulators 60 and 61,respectively, to solid-state radar T/R module 54. For an exemplary T/R module, + V1 is a pulsed voltage, and the remaining output voltages + V2 ... + Vn and - V2 . . . ---Vm are bias voltages

> used for control and receive functions. In operation, switching devices Qa and Qb are gated 180° out-of-phase with a 50% duty cycle by drive means 55. Hence, because one of the switching devices is always conducting, the energy-storage capacitor Ce is always transformer .. coupled to the positive and negative dc output buses.

We are unable to discern in this cited section where Steigerwald '090 teaches the urged swapping around the order and number of these specific components in the recited manner. It appears to us that the Requester has taken the isolated teaching of a discrete embodiment of Steigerwald '539 exchanging a MOSFET for a diode, and modified it with description from a different embodiment from Steigerwald '090, without an express or even implied disclosure of this modification.

We are in agreement with the position of the Patent Owner, that:

> [t]he assertion that Steigerwald '539 sets up an alternative embodiment as a modification to Steigerwald '090, Fig. 1 is contrary to the express purpose of both patents: which is primarily to supply the energy pulse for a radar T/R module (illustrated in Steigerwald '539, Fig. 2). The ordinary artisan could not reasonably conceive that the text of the Steigerwald '539 Patent could modify the later-filed Steigerwald '090 as asserted."

PO App. Br. 11.

Steigerwald '539, to the extent it is incorporated, is a separate, discrete embodiment and does not modify a later embodiment in Steigerwald '090.

In order for a reference to be anticipatory, it must disclose, either explicitly or implicitly, every element of the claim. See, *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986). As this combination does not, we reverse this rejection.

II. *The Rejection of Claims 24-26 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald 090.*

This rejection was adopted from the Request, pages 26-30. RAN 4. It extends the rejection to these dependent claims, which recite specific voltage levels, stating that the voltage levels would have been obvious. To the extent this rejection originates under a different statutory section, and there is some reasoning applicable under an obviousness standard as opposed to solely under an anticipation standard, we address this rejection below.

The Requester submitted the declaration of Dr. Patrizio Vinciarelli, which we have carefully reviewed. It states, from the indicated point of view of one of ordinary skill in the art, that:

(1) Steigerwald '090's basic teaching - to use a single non-regulating isolation stage to supply a multiplicity of non-isolating regulation stages so as to provide isolated and regulated power to multiple loads having different voltage requirements without multiple isolation stages - could be applied to any power system with a multiplicity of loads requiring different voltages. Such power systems are included computer and telecommunication equipment, in which digital logic circuits depend upon a multiplicity of different voltages on a common circuit board. Vinciarelli Declaration, para. 8.

(2) Steigerwald '090's teaching to use MOSFET synchronous rectifiers in some embodiments would be applicable, and advantageous, in any power system in which high efficiency was important, since synchronous rectifiers could be used to reduce the forward voltage drop and power loss that was inherent in diode rectifiers. In 1997, such power systems

included circuit boards for computer and telecommunication equipment. Vinciarelli Declaration, para. 9.

(3) In 1997, it was common for the main DC power bus in telecommunication equipment to have a voltage in the range of 36-75 volts (with a nominal level of 48 volts). Vinciarelli Declaration, para. 10.

(4) In 1997, it was common for different digital logic circuits to require power at 12V, 5V and 3.3V. Vinciarelli Declaration, para. 11.

The Requester urges, therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the Steigerwald conversion in electronic applications, and to use apply common voltages. Request 28.

There is not in our view a significant dispute in the record about above findings 3 and 4. We focus on findings 1 and 2, which are in dispute.

Patent Owner observes that Steigerwald '090 relates to a power converter with multiple output voltages to be applied to a phased array radar module. A goal of Steigerwald was to provide a power system of small volume. Schlecht Decl., para. 21; Dickens Decl., paras. 11-13. According to the Patent Owner, an energy storage capacitor connected to input terminals, rather than to the load terminals, can be of smaller size, because it is at a high voltage, and an isolation stage is used to reduce that voltage to a DC bus. The voltage on the DC bus is further reduced by series regulators, 50, 51, 60 and 61, which are illustrated in Steigerwald '090's Figure 1 as linear regulators.

The Patent Owner further points out that a feature of the Steigerwald '090 circuit was that there be no inductors in the current paths of the circuit. Patent Owner Response, January 17, 2012 at 8.

The Patent Owner further asserts that Steigerwald '090, in its attempt to make the power module have a very "small volume," Steigerwald '090, col. 1:37, operates at "high frequencies," Steigerwald '090, col. 3:24. As a result of the: 1) high-voltage energy storage capacitor instead of a low-voltage capacitor, 2) lack of series inductors and 3) high [switching] frequencies, the power module is small enough to "be embedded in the T/R module with the load ...," Steigerwald '090, col. 3:26-29. Moreover, Steigerwald '090 memorializes the lack of inductors in its claims, which recite a negative limitation multiple times.

We find we agree with the position of the Patent Owner that one of ordinary skill in the art would not be led, based upon Steigerwald '090 to modify it as the present rejection has done.

Of particular interest and persuasive value is the prosecution history of Steigerwald '090, which occurred long before this litigation and reexamination began:

> As amended, the claims are clearly patentable over the references. In short, Shimpo et al. describes a plurality of synchronized switching regulators. The claimed arrangement has no switching regulator at all; it has the switched capacitance multiplier, cascaded with linear voltage regulators. It is noted that such switching regulators include series inductors, which adversely affect the pulse response by their inductance, which introduces impedance into the current path. The switching regulator achieves its low output impedance by virtue of feedback, and the impedance rises as the frequency of the components of the pulse load increase, because the loop bandwidth decreases with increasing frequency. The claimed arrangement recites paths "without

> inductors" (although it is recognized that all paths may have some inherent inductance), to emphasize that the pulse operation is inherent in the low impedance of the recited structure over a substantial bandwidth.

Exh. 93, File History of Steigerwald '090, Amendment, May 19, 1994, page 6.

It is apparent from the above that avoidance of induction in the current path was critical to success in Steigerwald '090. Switching regulators would add inductance. We therefore disagree that one of ordinary skill in the art would do which is almost expressly excluded from the Steigerwald '090 reference, even though an alternative embodiment in Steigerwald '539 might seem to suggest a substitution in another location. That substitution is before the capacitance multiplier, and therefore the inductor would not be within the multiplied current path.

We agree with the Patent Owner's position in the response. January 17, 2012 Response, page 19. We expressly reject the Examiner's finding and conclusion that "it is eminently reasonable to believe that a person of ordinary skill in the art would see exactly how the converters of the '539 Patent relate to the converter of the '090 Patent." RAN 9. Rather, one of ordinary skill in the art would have recognized the problem with the substitution in the downstream location.

We also disagree with the underlying finding in the rejection that the reason for making the modifications is to improve efficiency. In the abstract, synchronous rectifiers can be thought of as increasing efficiency in some uses. However, we are persuaded that the embodiment of the '090 Patent could lose efficiency as a result of such a substitution. Among

other issues, the efficiency losses includes an increase in circuit complexity, loss in board space, increased cost due to the added gate control circuitry, and increased dissipation. *See*, e.g. the Schlecht Decl. Paras 27- 28.

Accordingly, we are persuaded that the cited references would not have been combined by one of ordinary skill in the art in the manner suggested by the Requester and adopted by the Examiner.

Moreover, even would one of ordinary skill in the art had a reason to combine the references, there is significant evidence of secondary considerations provided by the Patent Owner in the record. We must consider that and reweigh the ultimate conclusion as to whether the subject matter would have been patentable under 35 U.S.C. § 103.

In deciding questions of obviousness, we consider all four Graham factors including objective evidence of non-obviousness. A prima facie case made by the Examiner is not a conclusion on the ultimate issue of obviousness. The ultimate conclusion of obviousness is a legal conclusion to be reached after weighing all of the evidence on both sides. *Apple Inc. v. ITC*, 725 F.3d 1356, 1365 (Fed. Cir. 2013).

The Examiner stated that the evidence submitted was considered, but then adds the following comment:

> Patent Owner's response is heavily relied [sic – reliant?] on litigation evidence, which might or might not be the same evidence as in the court since Patent Owner is relying on the court itself as evidence. Patent Owner has repeatedly referred to alleged conclusions of the trial witnesses, the jury, and the District Court Judge without providing underlying evidence that these conclusions are allegedly based on. It is noted that the jury's verdict is not evidence and as stated in MPEP 2686 that Court decision will have no binding effect

> on the examination of the reexamination unless it is a final Court holding of claim invalidity/unenforceability.

RAN 7-8.

We disagree with this blanket statement that the affirmed adjudication of infringement cannot constitute informative or persuasive evidence of secondary considerations within the realm of making a patentability determination under § 103.

The '190 Patent was among those asserted in *SynQor, Inc. v. Artesyn Technologies, Inc. et al.*, No. 2:07-CV-497 (E.D. Tex.) against the Requester and others. After a jury trial, the Court enjoined the Defendants from infringement of the '190 Patent and others. PO App. Br. 1. Subsequently, the Court of Appeals for the Federal Circuit in a decision dated March 13, 2013, affirmed the decision of the Texas District Court. Appeal Nos. 2012-1069, -1070, -1071, and 1072. Additionally, the Federal Circuit denied the defendants' Petition for Rehearing and Rehearing En Banc on May 16, 2013. The Federal Circuit also denied the defendant's Motion to Stay the Mandate on May 28, 2013. The Mandate issued on May 30, 2013, making the Decision final. PO Reb. Br. 1.

Turning to the jury verdict form (Exhibit A20), we observe that the jury determined that (1) claims 2, 8, and 19 were infringed by the 42R8295 product of Bel Fuse and (2) Artesyn, Astec, Bel Fuse, Cherokee, Delta, Lineage, Murata, Murata Power Solutions, and Power One induced and contributed to infringement of claims 2, 8, 10, and 19. A20, pp. 9-26.

We are informed that millions of infringing units were sold, and that the end products are commensurate in scope with the instant claims. PO

Reb. Br. at 22-23 and 26-28. We are also informed that there is no substantially non-infringing use for the system, and conversely that there are no non-infringing alternatives, resulting in $80 million in lost profits to SynQor. *Id.* at 25. *See also* the Schlecht Declaration, A1, paras 59-63.

Returning to the claimed subject matter, claims 24, 25, and 26 depend from claim 20 and add particular voltage requirements.

Patent Owner argues that there is a nexus between the claims at issue and the objective evidence presented. PO App. Br. 23. Requester argues that the objective evidence should not be considered and is not convincing because unregulated intermediate bus architecture is not recited in the claims Resp. Br. 21.

We have, inter alia, reviewed the technical documents A 24-A75 and A105-201 which include data sheets for the various products found to infringe the '190 Patent.

As an example, we turn to Bel Fuse's product data sheets, documents A111 et seq. It is apparent that they describe products intended for configuration into a circuit such as that of claims 1 and 20. For example, 07CM-20S30S (A113) describes an unregulated output isolated bus converter "ideal for intermediate bus architecture" for powering multiple downstream non-isolated point-of-load converters Document A113, page 1. They deliver output voltages of 8 and 12 volts from a 48 volt input. *Id.* Instant claim 24 recites an input of 36 to 75 volts, and claim 25 recites an output of about 12 volts.

Our review of these documents, in conjunction with the District Court finding of infringement, contributory infringement, and/or induced

infringement of claims 2, 8, 10, and 19 of the '190 Patent and the jury award of lost profits suggest that claim 20, and its dependent claims, is reasonably commensurate in scope with the products at issue in the trial.

The fact that claims 1 and 20 do not recite the particular set of words "intermediate bus architecture" does not persuade us of a lack of nexus between the instant claims and the '497 litigation accused products. We therefore expressly disagree with the Examiner and Requester that the commercial success is lacking nexus. Resp. Br. 21.

The Patent Owner next argues that objective evidence establishes commercial success of the claimed invention. PO App. Br. 25. The Requester argues that the commercial success achieved by the '497 litigation defendants is not a result of the '190 Patent claimed subject matter because:

> Even with an intermediate bus, Unregulated IBA was spurred by evolving market forces that had nothing to do with the SynQor patents. In particular, the availability of low-cost, wide-input non-isolating Point of Load ("POL") converters was important for the use of the technique. As explained by Robert White in 2003, for example:
>
> > "The drivers for the wide adoption of the Intermediate Bus Architecture are: The large number of supply voltages needed in systems and on individual circuit cards in today's systems and the rapidly decreasing cost of nonisolated, point-of-Load (POL) dc-dc converters.
>
> For these reasons, the claims of the '190 Patent are not coextensive with products sold…

Resp. Br. 23.

The Patent Owner argues that devices covered by the claims replaced previous architectures used in high-end computers and telecommunication equipment, and the number of units sold by the '497 litigation defendants proves commercial success. The argument is supported by testimony from

various sources, including Dr. Schlecht (who we recognize has an interest in this proceeding, but note that the number of 2 million units initially sold and 5 million sold through trial is largely unrefuted). *See* Schlecht Declaration, Document A3, pages 2 et seq. Moreover, according to the Patent Owner, the '497 litigation infringing products constitute substantially the entire market. PO App. Br. 27.

Based on the evidence submitted at trial, it was established that the unregulated bus converters described in the defendants' data sheets have no substantial non-infringing use other than to create infringing unregulated intermediate bus architecture systems and that there are no suitable non-infringing alternatives to the infringing UIBA systems. On this basis, the jury awarded lost profits.

We are unpersuaded by the Requester's argument that the commercial success was due to the "unclaimed" unregulated intermediate bus architecture. Based on the above claim language, our analysis, and informed by the judgment and the analysis of the court, we find that the commercial success described by Patent Owner provides an objective indicia of non-obviousness, which would have been sufficient to overcome the Examiner's conclusion of obviousness .

We therefore reverse this rejection.

III. *The Rejection of Claims 1, 5-8, 11-13, 17, 18, 24, 28, and 31 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, and Cobos*

This rejection was adopted from the Request, pages 30-44. RAN 4.

The Request urges that Cobos teaches the importance of short transitions in the transformer voltage waveform where that waveform is used

to drive synchronous rectifiers. It also finds that Cobos provides motivation to modify Steigerwald '090 to add short transitions. Req. 31.

As Cobos does not rectify the deficiencies of the underlying Steigerwald references, we reverse this rejection for the reasons noted above.

IV. *The Rejection of Claims 2-4 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, Cobos, and Pressman.*

This rejection was adopted from the Request, pages 45-47. RAN 4.

As neither Cobos nor Pressman rectify the deficiencies of the underlying Steigerwald references, we reverse this rejection for the reasons noted above.

V. *The Rejection of Claims 9, 10, 14-16, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, and Cobos.*

This rejection was adopted from the Request, pages 47-52. RAN 5.

As Cobos does not rectify the deficiencies of the underlying Steigerwald references, we reverse this rejection for the reasons noted above.

VI. *The Rejection of Claims 1-33 under 35 U.S.C. § 103(a) as being unpatentable over Cobos and Pressman.*

This rejection was adopted from the Request, pages 53-80. RAN 5.

The Requester urged, and the Examiner adopted, findings that Cobos has a DC power source and all the elements of the non-regulating isolation stage of claim 1. According to the Requester and Examiner, Figure 5(b) of Cobos shows the transformer with primary and secondary windings, the two

synchronous converters driven by the secondary voltage waveform and thus synchronized with both the primary and secondary voltage waveforms synchronized with each other, and the optimum voltage waveform with short transitions as shown in Figure 5(c). Cobos is also said to describe a fixed duty cycle, i.e. a constant duty cycle 50% at page 1680. Request 53.

Cobos is found to be missing the non-isolating regulation stages driven by the output of the isolating stage. The Requester and Examiner rely on Pressman for a teaching of driving multiple non-isolated switching regulators from a single isolation stage. Specifically, they point to Figure 3-4(b) on page 82, with description on page 83. The motivation to make the combination is said to be to provide a multiplicity of different output voltages at high efficiency. The combination, the Examiner and Requester conclude, would have rendered claim 1 obvious to one of ordinary skill in the art at the time the invention was made. *Id*. at 54.

On the other side of the coin, the Patent Owner states that Cobos already provides a solution to providing a multiplicity of different output voltages at high efficiency in Figure 14(a), and the combination proposed by the Requester would not have high efficiency. PO Response, January 17, 2012, 39.

More specifically, it is urged that the solution of Cobos in Figure 14 (a) is said to be to use a plurality of half bridge circuits, each as shown in Figure 10, and each creating a different output at high efficiency. As noted at page 1680, left column, Figure 10 relies on variations in duty cycle to control the output voltage. Thus, the solution provided by Cobos is to

provide a plurality of high efficiency single-stage converters that both isolate and regulate.

Cobos is said to demonstrate efficiencies up to 90%. Cobos p. 1680. Thus, since Cobos had already presented a high efficiency solution to providing multiple output voltages, it is urged that the motivation suggested by the Requester does not exist.

Further, the Patent Owner asserts that Figure 3-4B of Pressman to which the Requester points has a very low efficiency relative to other circuits in Pressman or the one shown in Figure 14a of Cobos. The motivation of high efficiency suggested by Requester would not lead a person of ordinary skill to Figure 3-4B of Pressman. *Id.*

The Requester responds that Pressman expressly teaches that a non-regulating isolation stage such as the one found in Cobos can be used "to generate a multiplicity of different output voltages at high efficiency as shown in Fig. 3-4B." Resp. Br. 31. The Requester further urges that "Pressman also notes that the various components shown can be moved about in 'building block' fashion without unexpected results, and that there are many reasons to do so including, but certainly not limited to, efficiency." *Id.*

In rebuttal, the Patent Owner urges that Cobos teaches away from the proposed combination of references. Cobos is said to teach using a separate regulating isolation stage for each desired output voltage. "Cobos already presents a solution to achieve multiple output voltages, meaning there is

no reason to combine the references in the manner asserted by the [Requester], other than by impermissibly relying on SynQor's '190 patent claims as a guide in formulating the rejections." PO Reb. Br. 9.

The Patent Owner additionally notes that "Pressman also does not provide any reasoning or motivation to combine the references in the manner asserted by [Requester], specifically decrying the statement that circuit elements are 'building blocks' and that the building blocks can be recombined depending on the application." *Id.* (citing Pressman at 74).

On balance, we think the Patent Owner has the better argument. Without the guidance of the claims, one is left to move the building blocks of Pressman, a basic treatise, around in a random, albeit sometimes predictable, manner. As noted by the Patent Owner, Pressman generally provides no specific reasoning or motivation for combining any particular circuit elements in a particular configuration to create a specific circuit.

We also find merit to the Patent Owner's contention that Pressman's description of Figures 3-4(B) discusses that multiple output voltages may be obtained at high efficiency by using multiple switching post-regulators (one for each output) rather than series-pass post-regulators (which would result in low efficiency). We then are left principally with hindsight as the possible motivation for making this combination.

Moreover, the commercial success described by Patent Owner (and discussed above) provides an objective indicia of non-obviousness, which would have been sufficient to overcome the Examiner's conclusion of obviousness.

We therefore reverse this rejection as well.

VII. *The Rejection of Claims 34-38 under 35 U.S.C. § 103(a) as being unpatentable over Cobos and Pressman.*

This rejection was stated in the non-final action as adopted above against claims 1-33. RAN 5. Cobos in view of Pressman was applied as above to claims 1-33. Accordingly, as we have reversed that rejection (VI, above) and for the reasons stated above, we likewise reverse this rejection.

VIII. *The Rejection of Claims Claims 35-38 under 35 U.S.C. § 103(a) over Steigerwald '090, Steigerwald '539, Admitted Prior Art, and Pressman*

This rejection appears in the RAN at page 6. According to the Examiner, Steigerwald '090 and '539 (incorporated by reference) are applied as shown in the Non-Final Action against claims 20-23, 27, 29, 30, 32, and 33 (Section I above). New claims 35-38 are found to depend from claims 20 and 27 and claims 35 and 37 require switching regulators, whereas claims 36 and 38 require switching regulators, a DC power source providing a voltage within the range 36-75 volts wherein "the regulation stage output is of a voltage level to drive logic circuitry.

With regard to switching regulators, The Examiner found that Pressman teaches in connection with Figure 3-4B that the use of switching regulators "to generate a multiplicity of different output voltages" can achieve high efficiency. RAN 6.

The Examiner then concludes it would have been obvious to use the switching regulators of Pressman in the circuit of Steigerwald. *Id.*

Furthermore, the Examiner finds that limitations to an input voltage between 36 and 75 volts and an output voltage to drive logic circuitry are

Admitted Prior Art, citing to Dr. Schlecht's testimony and the background section of the '190 Patent. *Id.*

As this rejection depends upon the rejection in section I above which we have reversed, we reverse this rejection for those same reasons. Neither the Admitted Prior Art nor Pressman overcome the deficiencies of that rejection.

CONCLUSIONS

We have carefully considered the evidence of record, including that of secondary considerations submitted by the Patent Owner. We also have considered the evidence submitted by the Requester and the findings and conclusions of the Examiner. We conclude that a nexus exists between the claims under reexamination and the evidence of infringing products in the litigation.

The weight of the objective evidence, combined with the technical difficulties in implementing the proposed combinations of references adopted from the Request by the Examiner, lead us to the conclusion that the claims at issue would not have been obvious to one of only ordinary skill in the art at the time the invention was made.

The record does not establish that claims 1-38 would have been obvious to one of ordinary skill in the relevant art at the time of the effective date of the '190 Patent invention.

We, therefore, do not sustain any of the obviousness rejections of these claims.

ORDER

I. The rejection of claims 20-23, 27, 29, 30, 32 and 33 under 35 U.S.C. §102 (b) as anticipated by Steigerwald '090 and Steigerwald '539 is reversed.

II. The rejection of claims 24-26 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090 is reversed.

III. The rejection of claims 1, 5-8, 11-13, 17, 18, 24, 28, and 31 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, and Cobos is reversed.

IV. The rejection of claims 2-4 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, Cobos, and Pressman is reversed.

V. The rejection of claims 9, 10, 14-16, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Steigerwald '090, Steigerwald '539, and Cobos is reversed.

VI. The rejection of claims 1-33 under 35 U.S.C. § 103(a) as being unpatentable over Cobos and Pressman is reversed.

VII. The rejection of claims 34-38 under 35 U.S.C. § 103(a) as being unpatentable over Cobos and Pressman is reversed.

VIII. The rejection of claims 35-38 under 35 U.S.C. § 103(a) over Steigerwald '090, Steigerwald '539, Admitted Prior Art, and Pressman is reversed.

REVERSED

ak

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US007072190B2

(12) **United States Patent**
Schlecht

(10) **Patent No.: US 7,072,190 B2**
(45) **Date of Patent: Jul. 4, 2006**

(54) **HIGH EFFICIENCY POWER CONVERTER**

(75) Inventor: **Martin F. Schlecht**, Lexington, MA (US)

(73) Assignee: **SynQor, Inc.**, Boxborough, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/812,314**

(22) Filed: **Mar. 29, 2004**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Continuation of application No. 10/359,457, filed on Feb. 5, 2003, now Pat. No. 6,731,520, which is a continuation of application No. 09/821,655, filed on Mar. 29, 2001, now Pat. No. 6,594,159, which is a division of application No. 09/417,867, filed on Oct. 13, 1999, now Pat. No. 6,222,742, which is a division of application No. 09/012,475, filed on Jan. 23, 1998, now Pat. No. 5,999,417.

(60) Provisional application No. 60/036,245, filed on Jan. 24, 1997.

(51) **Int. Cl.**
H02M 3/335 (2006.01)

(52) **U.S. Cl.** **363/21.06**

(58) **Field of Classification Search** 363/15–17, 363/21.06, 21.14, 56.01, 56.02, 95, 97, 98, 363/131, 132
See application file for complete search history.

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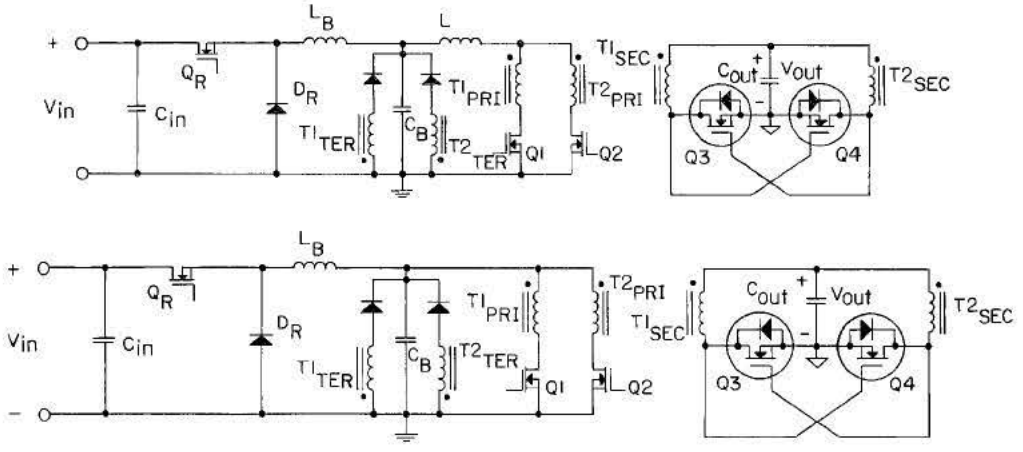
Primary Examiner—Matthew V. Nguyen
(74) *Attorney, Agent, or Firm*—Hamilton, Brook, Smith & Reynolds, P.C.

(57) **ABSTRACT**

A power converter nearly losslessly delivers energy and recovers energy from capacitors associated with controlled rectifiers in a secondary winding circuit, each controlled rectifier having a parallel uncontrolled rectifier. First and second primary switches in series with first and second primary windings, respectively, are turned on for a fixed duty cycle, each for approximately one half of the switching cycle. Switched transition times are short relative to the on-state and off-state times of the controlled rectifiers. The control inputs to the controlled rectifiers are cross-coupled from opposite secondary transformer windings.

33 Claims, 7 Drawing Sheets



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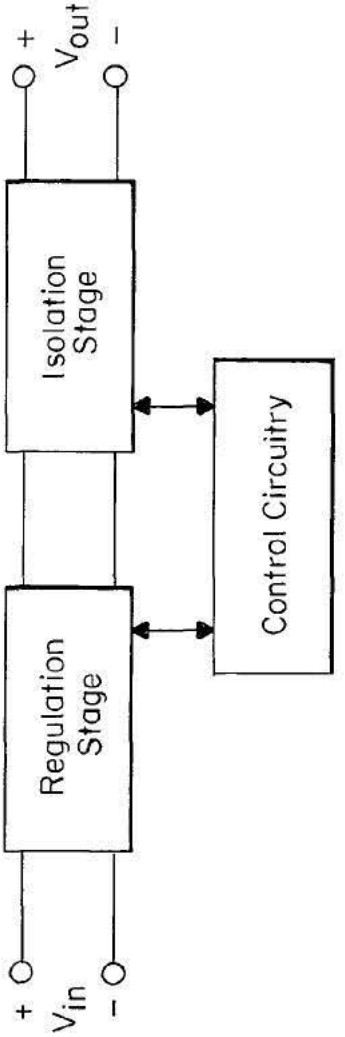
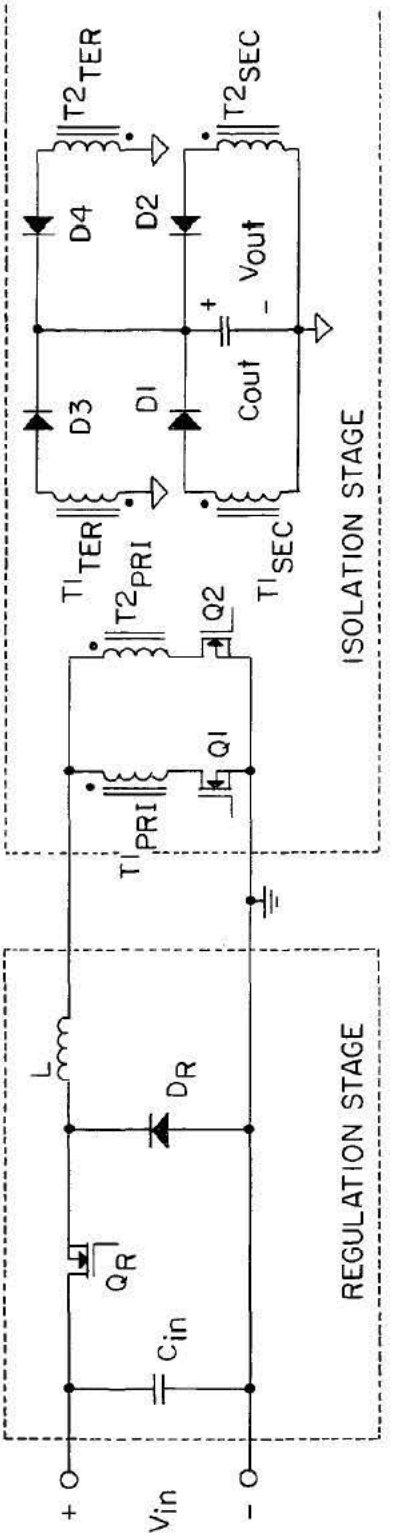

+
Vout
−
Isolation Stage
Regulation Stage
Control Circuitry
+
Vin
−

FIG. 1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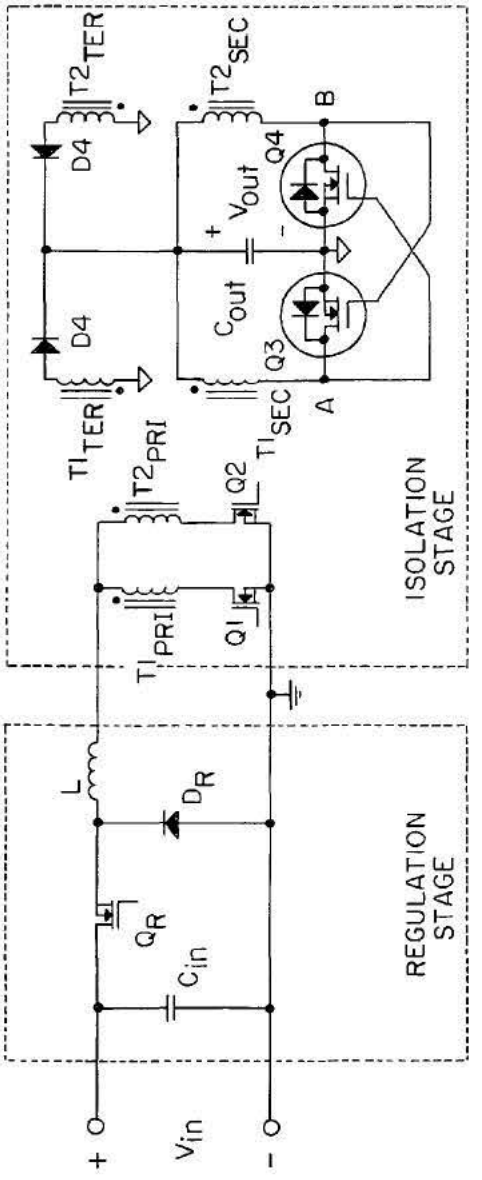
D4
D2
Vout
D3
DI
Cout
T1TER
T2PRI
Q2
T1SEC
ISOLATION STAGE
T1PRI
QI
L
DR
QR
Cin
REGULATION STAGE
+
Vin
−

FIG. 2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D4
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Q4
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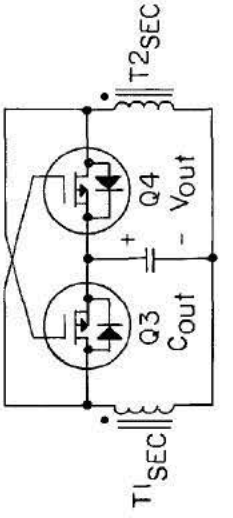
+
-
Cout
Q3
A
TITER
T2PRI
Q2
TISEC
TIPRI
Q1
ISOLATION STAGE
L
DR
QR
Cin
REGULATION STAGE
+
Vin
-

FIG. 3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+
Vout
-
Q3
Cout
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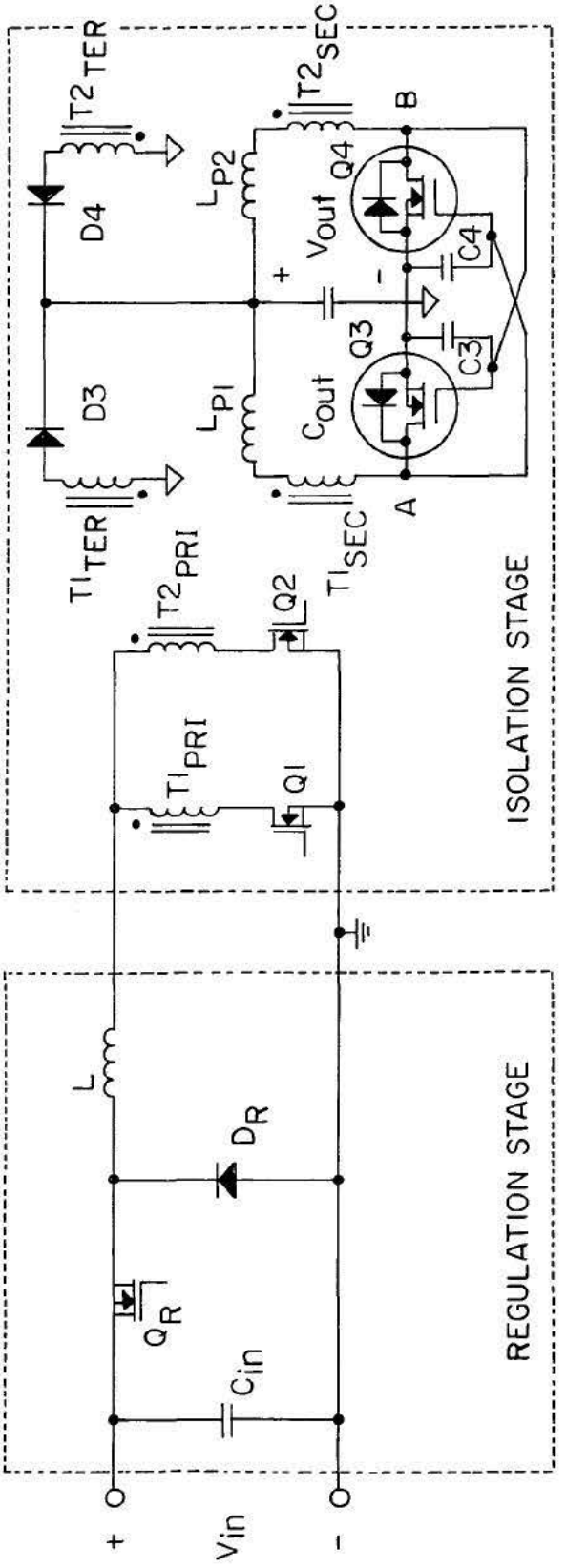
FIG. 4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Vout
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C4
D3
LPI
Cout
Q3
C3
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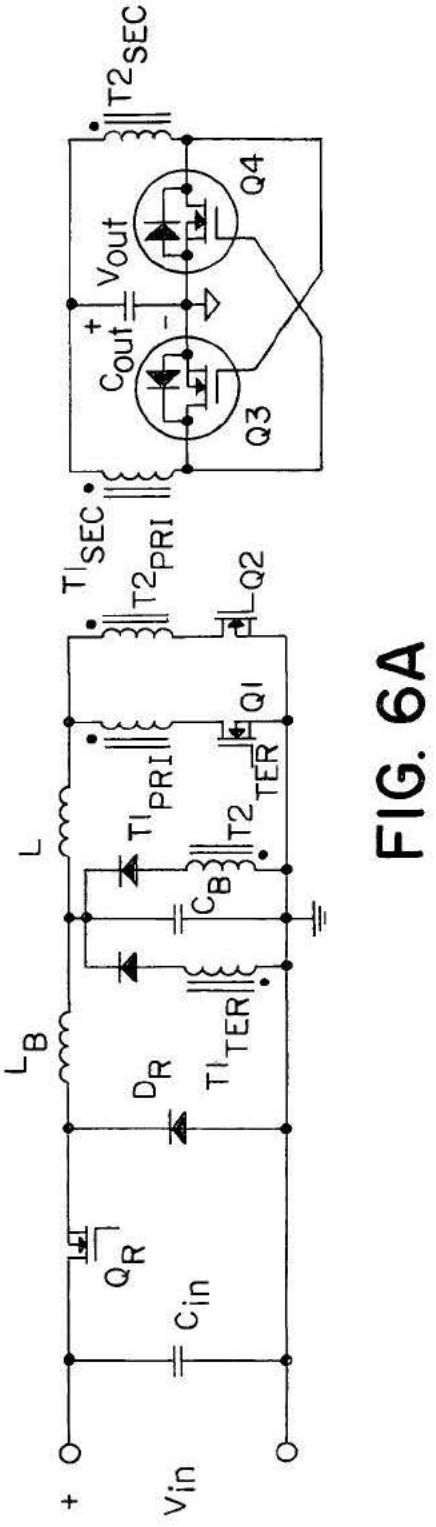
T1 SEC
A
T2 PRI
Q2
T1 PRI
QI
ISOLATION STAGE
L
DR
QR
Cin
REGULATION STAGE
+
Vin
-

FIG. 5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Q1
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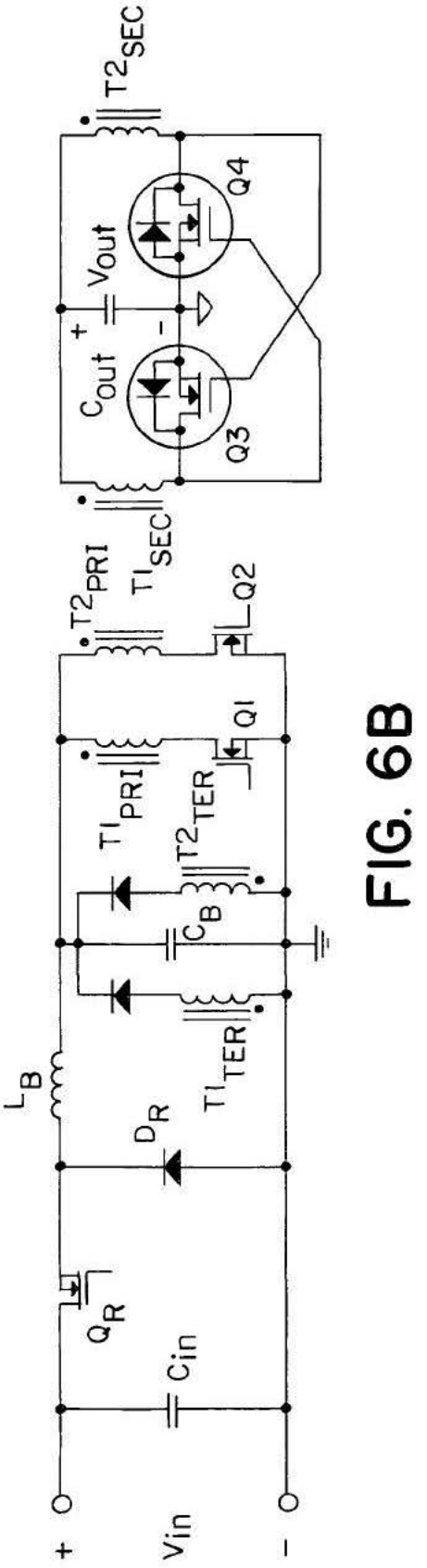
LB
DR
QR
Cin
Vin
+

FIG. 6A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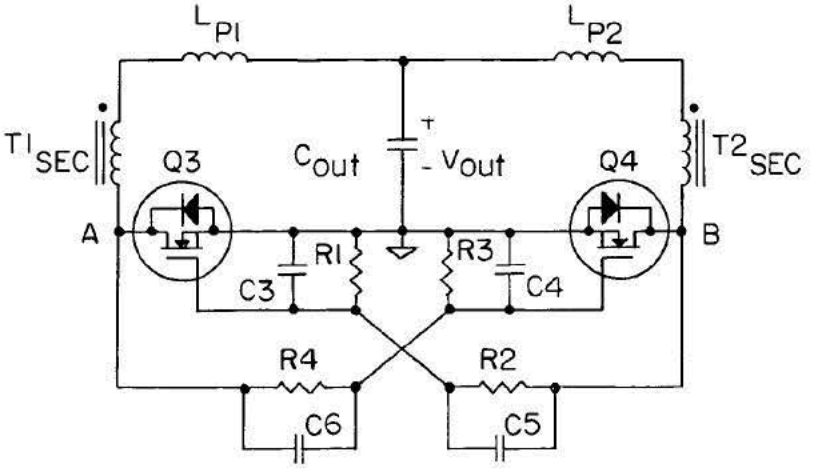
DR
QR
Cin
Vin
+
-

FIG. 6B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L P2
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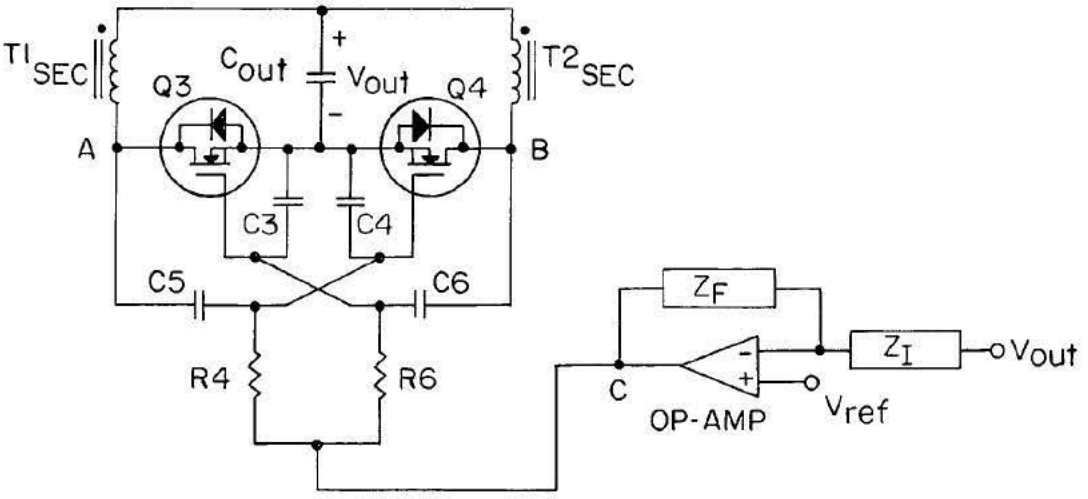
T2 SEC
Q3
Q4
C out
+
- V out
A
B
R1
R3
C3
C4
R4
R2
C6
C5

FIG. 7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Q4
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+
V out
-
A
B
C3
C4
C5
C6
R4
R6
Z F
Z I
V out
C
OP-AMP
V ref

FIG. 8

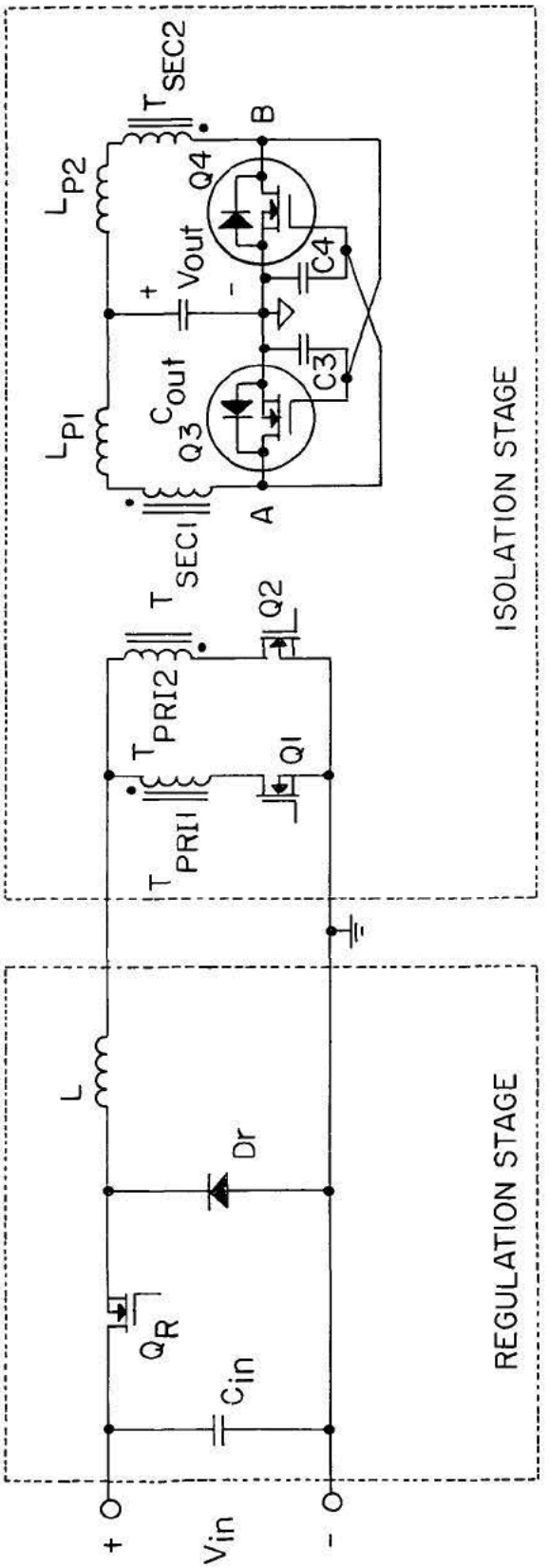

ISOLATION STAGE
REGULATION STAGE
T SEC2
B
L P2
Q4
Vout
C4
C3
C out
Q3
L PI
T SEC1
A
Q2
T PRI2
T PRI1
QI
L
Dr
QR
Cin
+
Vin
-

FIG. 9

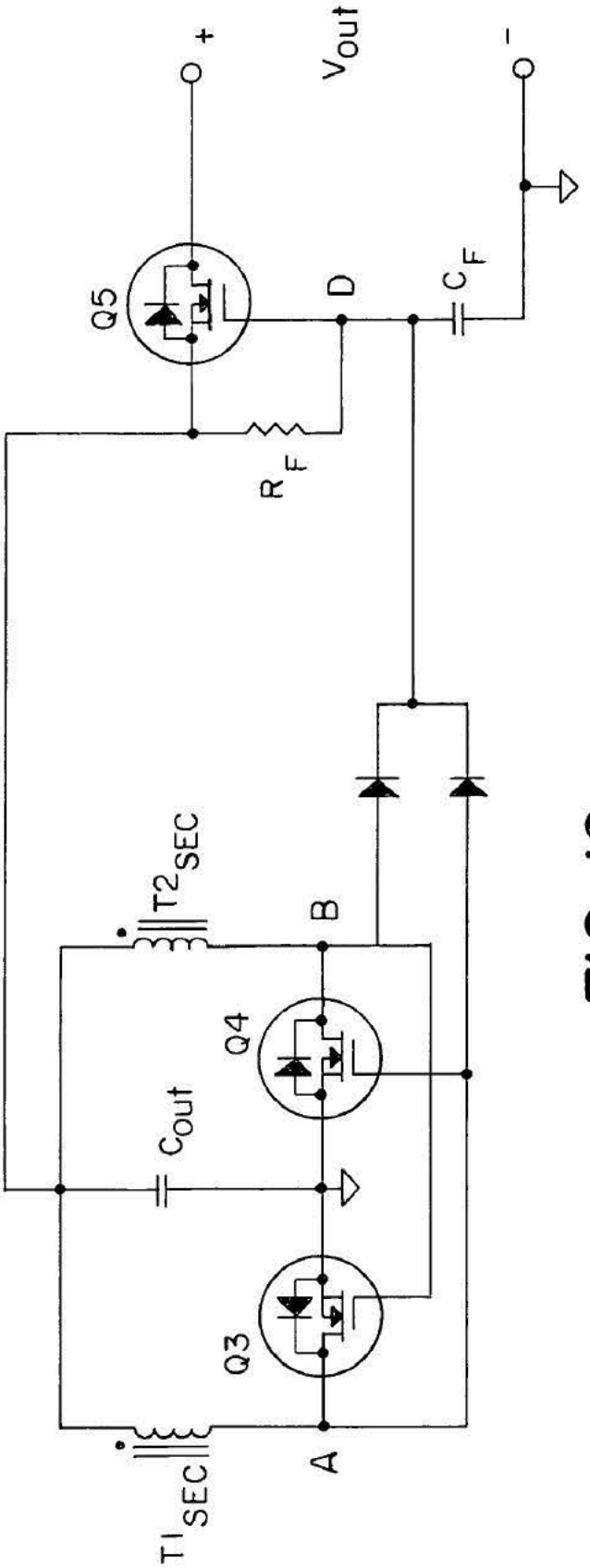


FIG. 10

HIGH EFFICIENCY POWER CONVERTER

RELATED APPLICATIONS

This application is a continuation of application Ser. No. 10/359,457, filed Feb. 5, 2003, now U.S. Pat. No. 6,731,520 which continuation of application Ser. No. 09/821,655, filed Mar. 29, 2001, now U.S. Pat. No. 6,594,159, which is a divisional of application Ser. No. 09/417,867, filed Oct. 13, 1999, now U.S. Pat. No. 6,222,742, which is a divisional of Ser. No. 09/012,475, filed Jan. 23, 1998, now U.S. Pat. No. 5,999,417, which claims the benefit of U.S. Provisional Application 60/036,245 filed Jan. 24, 1997. The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

This invention pertains to switching power converters. A specific example of a power converter is a DC-DC power supply that draws 100 watts of power from a 48 volt DC source and converts it to a 5 volt DC output to drive logic circuitry. The nominal values and ranges of the input and output voltages, as well as the maximum power handling capability of the converter, depend on the application.

It is common today for switching power supplies to have a switching frequency of 100 kHz or higher. Such a high switching frequency permits the capacitors, inductors, and transformers in the converter to be physically small. The reduction in the overall volume of the converter that results is desirable to the users of such supplies.

Another important attribute of a power supply is its efficiency. The higher the efficiency, the less heat that is dissipated within the supply, and the less design effort, volume, weight, and cost that must be devoted to remove this heat. A higher efficiency is therefore also desirable to the users of these supplies.

A significant fraction of the energy dissipated in a power supply is due to the on-state (or conduction) loss of the diodes used, particularly if the load and/or source voltages are low (e.g. 3.3, 5, or 12 volts). In order to reduce this conduction loss, the diodes are sometimes replaced with transistors whose on-state voltages are much smaller. These transistors, called synchronous rectifiers, are typically power MOSFETs for converters switching in the 100 kHz and higher range.

The use of transistors as synchronous rectifiers in high switching frequency converters presents several technical challenges. One is the need to provide properly timed drives to the control terminals of these transistors. This task is made more complicated when the converter provides electrical isolation between its input and output because the synchronous rectifier drives are then isolated from the drives of the main, primary side transistors. Another challenge is the need to minimize losses during the switch transitions of the synchronous rectifiers. An important portion of these switching losses is due to the need to charge and discharge the parasitic capacitances of the transistors, the parasitic inductances of interconnections, and the leakage inductance of transformer windings.

SUMMARY OF THE INVENTION

Various approaches to addressing these technical challenges have been presented in the prior art, but further improvements are needed. In response to this need, a new power circuit topology designed to work with synchronous rectifiers in a manner that better addresses the challenges is presented here.

In preferred embodiments of the invention, a power converter comprises a power source and a primary transformer winding circuit having at least one primary winding connected to the source. A secondary transformer winding circuit has at least one secondary winding coupled to the at least one primary winding. Plural controlled rectifiers, such as voltage controlled field effect transistors, each having a parallel uncontrolled rectifier, are connected to a secondary winding. Each controlled rectifier is turned on and off in synchronization with the voltage waveform across a primary winding to provide an output. Each primary winding has a voltage waveform with a fixed duty cycle and transition times which are short relative to the on-state and off-state times of the controlled rectifiers. A regulator regulates the output while the fixed duty cycle is maintained.

In the preferred embodiments, first and second primary transformer windings are connected to the source and first and second primary switches are connected in series with the first and second primary windings, respectively. First and second secondary transformer windings are coupled to the first and second primary windings, respectively. First and second controlled rectifiers, each having a parallel uncontrolled rectifier, are in series with the first and second secondary windings, respectively. A controller turns on the first and second primary switches in opposition, each for approximately one half of the switching cycle with transition times which are short relative to the on-state and off-state times of the first and second controlled rectifiers. The first and second controlled rectifiers are controlled to be on at substantially the same times that the first and second primary switches, respectively, are on.

In a system embodying the invention, energy may be nearly losslessly delivered to and recovered from capacitors associated with the controlled rectifiers during their transition times.

In the preferred embodiments, the first primary and secondary transformer windings and the second primary and secondary transformer windings are on separate uncoupled transformers, but the two primary windings and two secondary windings may be coupled on a single transformer.

Preferably, each controlled rectifier is turned on and off by a signal applied to a control terminal relative to a reference terminal of the controlled rectifier, and the reference terminals of the controlled rectifiers are connected to a common node. Further, the signal that controls each controlled rectifier is derived from the voltage at the connection between the other controlled rectifier and its associated secondary winding.

Regulation may be through a separate regulation stage which in one form is on the primary side of the converter as part of the power source. Power conversion may then be regulated in response to a variable sensed on the primary side of the converter. Alternatively, the regulator may be a regulation stage on the secondary side of the converter, and power conversion may be regulated by control of the controlled rectifiers. Specifically, the on-state voltage of a controlled rectifier may be made larger than its minimum value to provide regulation, or the on-state duration of a controlled rectifier may be shorter than its maximum value to provide regulation.

The preferred systems include reset circuits associated with transformers for flow of magnetizing current. The energy stored in the magnetizing inductance may be recov-

ered. In one form, the reset circuit comprises a tertiary transformer winding, and in another form it comprises a clamp.

In preferred embodiments, the power source has a current fed output, the current fed output characteristic of the power source being provided by an inductor. Alternatively, the power source may have a voltage-fed output where the voltage-fed output characteristic of the power source is provided by a capacitor. In either case, the characteristics may alternatively be provided by active circuitry.

With the preferred current-fed output, the primary switches are both turned on during overlapping periods, and the overlapping periods may be selected to achieve maximum efficiency. With the voltage-fed output, the primary switches are both turned off during overlapping periods. Additional leakage or parasitic inductance may be added to the circuit to accommodate an overlap period.

In one embodiment, a signal controlling a controlled rectifier is derived with a capacitive divider circuit. A circuit may determine the DC component of the signal controlling the controlled rectifier, and the DC component of the signal may be adjusted to provide regulation.

In accordance with another aspect of the invention, an ORing controlled rectifier connects the converter's output to an output bus to which multiple converter outputs are coupled, and the ORing controlled rectifier is turned off if the power converter fails. Preferably, the signal controlling the ORing controlled rectifier is derived from one or more secondary windings. The ORing controlled rectifier is turned on when the converter's output voltage approximately matches the bus voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

FIG. **1** is a block diagram illustrating a preferred embodiment of the invention.

FIG. **2** is a schematic of an embodiment of the invention with synchronous rectifiers replaced by diodes.

FIG. **3** is an illustration of a preferred embodiment of the invention with the controlled rectifiers and parallel uncontrolled rectifiers illustrated.

FIG. **4** illustrates an alternative location of the synchronous rectifiers in the circuit of FIG. **3**.

FIG. **5** illustrates the circuit of FIG. **3** with important parasitic capacitances and inductances illustrated.

FIG. **6**A illustrates another embodiment of the invention with the tertiary winding connected to the primary side.

FIG. **6**B illustrates another embodiment of the invention with a voltage fed isolation stage.

FIG. **7** illustrates a secondary circuit having capacitive dividers to divide the voltages applied to the control terminals of the controlled rectifiers.

FIG. **8** shows an alternative embodiment in which the output is regulated by controlling the voltage applied to the control terminals of the controlled rectifiers.

FIG. **9** illustrates an embodiment of the invention in which the primary windings are tightly coupled.

FIG. **10** illustrates the use of an ORing controlled rectifier to couple the power converter to an output bus.

DETAILED DESCRIPTION OF THE INVENTION

A description of preferred embodiments of the invention follows.

One embodiment of the invention described herein pertains to an electrically isolated DC-DC converter that might be used to deliver power at a low DC voltage (e.g. 5 volts) from a DC source such as a battery or a rectified utility. In such a converter a transformer is used to provide the electrical isolation and to provide a step-down (or step-up) in voltage level according to its turns-ratio. Switches in the form of power semiconductor transistors and diodes are used in conjunction with capacitors and inductors to create the conversion. A control circuit is typically included to provide the drive signals to the transistors' control terminals.

When the switching frequency is high (e.g. 100 kHz and above) it is typical today to use power MOSFETs and Schottky diodes for the converter's switches since these majority carrier devices can undergo faster switch transitions than minority carrier devices such as power bipolar transistors and bipolar diodes.

Most DC-DC converters are designed to provide regulation of their output voltage in the face of input voltage and output current variations. For example, a converter might need to maintain a 5 volt output (plus or minus a few percent) as its input varies over the range of 36 to 75 volts and its output current ranges from 1 to 25 amps. This ability to provide regulation is usually the result of the power circuit's topology and the manner in which its switching devices are controlled. Sometimes the regulation function is supplied by (or augmented with) a linear regulator.

FIG. **1** shows a block diagram of a DC-DC converter that represents one embodiment of the invention. It shows a two stage converter structure where the power first flows through one stage and then through the next. One stage provides the regulation function and the other provides the electrical isolation and/or step-down (or step-up) function. In this embodiment the regulation stage is situated before the isolation stage, but this ordering is not necessary for the invention. Notice also that the block diagram shows a control function. As mentioned, the purpose of this control function is to determine when the transistors in the power circuit will be turned on and off (or to determine the drive of a linear regulator). To aid in this function the control circuit typically senses voltages and currents at the input, at the output, and/or within the power circuit.

FIG. **2** shows one way to implement the two power stages represented in the block diagram of FIG. **1**. In this figure diodes, rather than synchronous rectifiers, are used to simplify the initial description of the circuit's operation. The topology of the regulation stage is that of a "down converter". This canonical switching cell has a capacitor, C_{IN}, a transistor, Q_R, a diode, D_R, and an inductor, L. Regulation is by control of the duty cycle of the transistor Q_R in response to one or more parameters sensed in the circuit. In a well known manner the regulation stage can be modified by providing higher order filters at its input and output, by replacing the diode with a synchronous rectifier, by adding resonant elements to create a "multi-resonant" converter and the like.

The topology of the isolation stage shown in FIG. **2** has two transformers that are not, in this case, coupled. Each of these transformers T**1** and T**2** has three windings: a primary winding $T1_{PRI}$, $T2_{PRI}$; a secondary winding $T1_{SEC}$, $T2_{SEC}$; and a tertiary winding $T1_{TER}$, $T2_{TER}$. The transformer windings are connected through MOSFETs Q**1** and Q**2** on the

primary windings and through diodes D1, D2, D3, and D4 on the secondary and tertiary windings. The stage is "current-fed", in this case by the inductor L from the output of the regulation stage. By this it is meant that the current flowing into the primary side of the isolation stage is held relatively constant over the time frame of the switching cycle. It also means that the voltage across the primary side of the isolation stage is free to have large, high frequency components. The output filter is simply a capacitor C_{OUT} whose voltage is relatively constant over the time frame of the switching cycle. Additional filtering stages could be added to this output filter in a known manner.

The operation of the isolation stage proceeds in the following manner. First, for approximately one half of the switching cycle, transistor Q1 is on and Q2 is off. The current flowing through inductor L therefore flows through the primary winding of transformer T1 , and a corresponding current (transformed by the turns ratio) flows through the secondary winding of T1 and through diode D1 to the output filter capacitor C_{OUT} and the load. During this time the magnetizing current in T1 is increasing due to the positive voltage placed across its windings. This positive voltage is determined by the output capacitor voltage, V_{OUT}, plus the forward voltage drop of D1.

During the second half of the switching cycle, transistor Q2 and diode D2 are on and Q1 and D1 are off. While the current of inductor L flows through transformer T2 in the same manner as described above for T1, the magnetizing current of transformer T1 flows through its tertiary winding and diode D3 to the output filter capacitor, C_{OUT}. This arrangement of the tertiary winding provides a means to reset the T1 transformer core with a negative voltage and to recover most of the magnetizing inductance energy. The tertiary winding may alternatively be connected to other suitable points in the power circuit, including those on the primary side of the transformer.

Other techniques for resetting the core and/or for recovering the magnetizing energy are known in the art and may be used here. In particular, the tertiary winding could be eliminated and replaced with a conventional clamp circuit attached to either the primary or secondary winding and designed to impose a negative voltage across the transformer during its operative half cycle. Techniques to recover the energy delivered to this clamp circuit, such as the one in which a transistor is placed in anti-parallel with a clamping diode so that energy can flow from the clamping circuitry back into the magnetizing inductance, could also be used.

Notice that because the isolation stage of FIG. 2 is fed by an inductor (L), it is important to make sure there is at least one path through which the current in this inductor can flow. At the transitions between each half cycle, it is therefore typical to turn on the new primary side transistor (say Q2) before turning off the old primary side transistor (say Q1). The time when both transistors are on will be referred to as an overlap interval.

In a conventional current-fed push-pull topology where all the transformer windings are coupled on a single core, turning on both primary-side transistors will cause the voltage across the transformer windings to drop to zero, the output diodes to turn off, and the power to stop flowing through the isolation stage.

Here, however, since two separate, uncoupled transformers are used, the voltage across the transformer windings does not have to collapse to zero when both Q1 and Q2 are on. Instead, both of the output diodes D1 and D2 turn on, both transformers have a voltage across them determined by the output voltage, and the current of inductor L splits (not necessarily equally) between the two halves of the isolation stage. The power flow through the isolation stage is therefore not interrupted (except to charge/discharge parasitic capacitances and inductances). This means the output filter (C_{OUT}) can be made much smaller and simpler than would otherwise be necessary. It also means that the isolation stage does not impose a large fundamental frequency voltage ripple across the inductor (L) which provides its current-fed input characteristic.

After an appropriate amount of overlap time has elapsed, the old primary side transistor (say Q1) is turned off. The voltage across this transistor rises as its parasitic capacitance is charged by the current that had been flowing through the channel. Once this voltage rises high enough to forward bias diode D3 connected to the tertiary winding, the transistor voltage becomes clamped, although an over-ring and/or a commutation interval will occur due to parasitic leakage inductance. Eventually, all of the current in inductor L will flow through switch Q2, switch Q1 will be off, and the magnetizing current of T1 will flow through diode D3.

Now replace output diodes D1 and D2 with MOSFET synchronous rectifiers Q3 and Q4, as shown in FIG. 3. Note that in this and later figures, the body diode of the MOSFET synchronous rectifier is explicitly shown since it plays a role in the circuit's operation. More generally, the schematical drawings of Q3 and Q4 depict the need for a controlled rectifier (e.g. a transistor) and an uncontrolled rectifier (e.g. a diode) connected in parallel. These two devices may be monolithically integrated, as they are for power MOSFETs, or they may be separate components. The positions of these synchronous rectifiers in the circuit are slightly different than the positions of the diodes in FIG. 2. They are still in series with their respective secondary windings, but are connected to the minus output terminal rather than the positive output terminal. This is done to have the sources of both N-channel MOSFETs connected to a single, DC node. If P-channel MOSFETs are to be used, their position in the circuit would be as shown in the partial schematic of FIG. 4. This position permits the P-channel devices to also have their sources connected to a single, DC node.

As shown in FIG. 3, the gates of the synchronous rectifier MOSFETs are cross-coupled to the opposite transformers. With this connection, the voltage across one transformer determines the gate voltage, and therefore the conduction state (on or off) of the MOSFET connected to the other transformer, and vice versa. These connections therefore provide properly timed drives to the gates of the MOSFETs without the need for special secondary side control circuitry.

For instance, during the half cycle in which transistor Q1 is turned on and transistor Q2 is off, the current of inductor L flows into the primary of T1 and out its secondary. This secondary side current will flow through transistor Q3 (note that even if Q3's channel is not turned on, the secondary side current will flow through the transistor's internal anti-parallel body diode). The voltage across transformer T1's secondary winding is therefore positive, and equal to the output voltage V_{OUT} plus the voltage drop across Q3. The voltage across T2's secondary winding is negative during this time, with a magnitude approximately equal to the output voltage if the magnetizing inductance reset circuitry takes approximately the whole half cycle to finish its reset function. (The negative secondary winding voltage may be made greater than the positive voltage so that the core will finish its reset before the next half cycle begins. This could be accomplished, for example, by using less turns on the tertiary winding.)

Referring to FIG. **3**, the voltage at node A during this state of operation is nearly zero with respect to the indicated secondary-side ground node (actually the voltage is slightly negative due to the drop across Q**3**). The voltage at node B, on the other hand, is, following our example, approximately twice the output voltage (say 10 volts for a 5 volt output). Given the way these nodes are connected to the synchronous rectifier transistors, Q**3** is turned on and Q**4** is turned off. These respective conduction states are consistent with transformer T**1** delivering the power and transformer T**2** being reset.

In the second half-cycle when Q**2** is on and Q**1** is off, the voltage at node B will be nearly zero (causing Q**3** to be off) and the voltage at node A will be approximately twice the output voltage (causing Q**4** to be on).

During the transition from one half-cycle to the next, the sequence of operation is as follows. Start with Q**1** and Q**3** on, Q**2** and Q**4** off. (The clamp circuit's diode D**4** may still be on, or it may have stopped conducting at this point if the magnetizing inductance has finished resetting to zero.) First, Q**2** is turned on. If we ignore the effects of parasitic capacitances and inductances, the voltage across T**2** steps from a negative value to a positive value. The current flowing through inductor L splits between the two primary windings, causing current to flow out of both secondary windings. These secondary currents flow through Q**3** and Q**4**. Since the voltages at both node A and node B are now nearly zero, Q**3**, which was on, will now be off, and Q**4** will remain off (or more precisely, the channels of these two devices are off). The secondary side currents therefore flow through the body diodes of Q**3** and Q**4**.

At the end of the overlap interval, Q**1** is turned off. The current stops flowing through transformer T**1**, the body diode of Q**3** turns off, and the voltage at node A rises from nearly zero to approximately twice the output voltage as T**1** begins its reset half-cycle. With node A voltage high, the channel of transistor Q**4** turns on, and the secondary side current of transformer T**2** commutates from the body diode of Q**4** to its channel.

Notice that during the overlap interval, the secondary side currents flow through the body diodes of transistors Q**3** and Q**4**, not their channels. Since these diodes have a high on-state voltage (about 0.9V) compared to the on-state voltage of the channel when the gate-source voltage is high, a much higher power dissipation occurs during this interval. It is therefore desirable to keep the overlap interval short compared to the period of the cycle.

Notice also the benefit of using two, uncoupled transformers. The voltage across a first transformer can be changed, causing the channel of the MOSFET synchronous rectifier transistor connected to a second transformer to be turned off, before the voltage across the second transformer is made to change. This could not be done if both primary and both secondary windings were tightly coupled in the same transformer, since the voltages across all the windings would have to change together.

FIG. **5** shows the same topology as FIG. **3**, but with several important parasitic capacitances and inductances indicated schematically. Each indicated capacitor (C**3** and C**4**) represents the combined effect of one synchronous rectifier's input capacitance and the other rectifier's output capacitance, as well as other parasitic capacitances. Each indicated inductor (L_{P1}, and L_{P2}) represents the combined effect of a transformer leakage inductance and the parasitic inductance associated with the loops formed by the primary side components and the secondary side components. These elements store significant energy that is dissipated each switching cycle in many prior art power circuits where diodes are replaced with synchronous rectifiers. Here, however, the energy stored in these parasitic components is nearly losslessly delivered to and recovered from them. By nearly lossless it is meant that no more than approximately 30% of the energy is dissipated. With one implementation of the present invention, less than 10% dissipation is obtained.

The nearly lossless delivery and recovery of energy is achieved because the circuit topology permits the synchronous rectifier switch transitions to proceed as oscillations between inductors and capacitors. These transitions are short compared to the overall on-state and off-state portions of the switching cycle (e.g. less than 20% of the time is taken up by the transition). This characteristic of nearly lossless and relatively short transitions, which we will call soft switching, is distinct from that used in full resonant, quasi-resonant, or multi-resonant converters where the oscillations last for a large portion, if not all, of the on-state and/or off-state time.

The way in which the soft-switching characteristic is achieved can be understood in the following manner. Start with transistors Q**1** and Q**3** on, Q**2** and Q**4** off. The voltage at node A, and therefore the voltage across C**4**, is nearly zero and the voltage at node B (and across C**3**) is approximately twice the output voltage. The current flowing through inductor L, I_L, is flowing into the primary winding of T**1**. The current flowing out of the secondary winding of T**1** is I_L minus the current flowing in TI's magnetizing inductance, I_M, both referenced to the secondary side. The magnetizing current is increasing towards its maximum value, I_{MPK}, which it reaches at the end of the half cycle.

When Q**2** is turned on at the end of the half cycle, the voltage across both windings of both transformers steps to zero volts in the circuit model depicted in FIG. **5**. An L-C oscillatory ring ensues between capacitor C**3** and the series combination of the two parasitic inductances, L_{P1}, and L_{P2}. If we assume the parasitic capacitances and inductances are linear, the voltage across C**3** decreases cosinusoidally toward zero while the current flowing out of the dotted end of T**2**'s secondary winding, I_{LP2}, builds up sinusoidally toward a peak determined by the initial voltage across C**3** divided by the characteristic impedance

$$\sqrt{\frac{L_{P1}+L_{P2}}{C_3}}.$$

Note that the current flowing out of the dotted end of T**1**'s secondary winding, I_{LP1}, decreases by the same amount that I_{LP2} increases such that the sum of the two currents is (I_L-I_{MPK}), referenced to the secondary side. Also note that during this part of the transition, the voltages across both transformers' secondary windings will be approximately the output voltage minus half the voltage across C**3**. As the oscillation ensues, therefore, the transformer winding voltages, which started at zero, build up toward the output voltage.

The oscillation described above will continue until either the current I_{LP2} reaches (I_L-I_{MPK}) or the voltages across C**3** reaches zero. The first scenario occurs for lower values of (I_L-I_{MPK}) and the second occurs for higher values of this current.

If I_{LP2} reaches (I_L-I_{MPK}) first (and assuming the voltage across C**3** has fallen below the threshold voltage of Q**3** so that I_{LP1} is flowing through the body diode of Q**3**), the

oscillation stops because the body diode will not let I_{LP1} go negative. I_{LP2} and I_{LP1} will hold constant at (I_L-I_{MPK}) and zero, respectively. Whatever voltage remains across C3 will then discharge linearly due to the current I_{LP2} until the body diode of Q4 turns on. The body diode will then carry I_{LP2} until the overlap interval is over and Q1 is turned off.

When Q1 is turned off, the magnetizing current I_{MPK} will charge the parallel capacitance of C4 and C1, the parasitic output capacitance of Q1, until the voltage across them is high enough to forward bias the clamping diode D3. At this point the reset portion of T1's cycle commences.

Notice that for this first scenario, the complete transition is accomplished with portions of oscillatory rings that, to first order, are lossless. (Some loss does occur due to parasitic series resistance, but this is generally less than 20% of the total energy and typically around 5%.) It could be said that the energy that had been stored in L_{P1} has been transferred to L_{P2}, and that the energy that had been stored in C3 has been transferred to C4.

If, on the other hand, the voltage across C3 reaches zero (or, more precisely, a diode drop negative) first, then the body diode of Q4 will turn on and prevent this voltage from ringing further negative. The currents I_{LP1} and I_{LP2} (which are flowing through the body diodes of Q3 and Q4) will hold constant until the overlap interval is over and Q1 is turned off.

Once Q1 is turned off, an oscillation ensues between L_{P1}, and C1. This oscillation is driven by the current remaining in L_{P1}, when Q1 was turned off. Given typical parameter values, this oscillation will continue until I_{LP1} reaches zero, at which point the body diode of Q3 will turn off. Finally, the magnetizing current I_{MPK} charges up the parallel combination of C4 and C1 until the clamping diode D3 turns on to start the reset half-cycle.

Notice that for this second scenario, the transition is almost accomplished in a (to first order) lossless manner. Some loss does occur because in the final portion of the transition the voltages across C4 and C1 do not start out equal. C1 has already been partially charged whereas C4 is still at zero volts. As these capacitor voltages equalize, an energy will be lost. This lost energy is a small fraction (typically less than one third) of the energy stored in C1 before the equalization occurs. The energy stored in C1 equals the energy stored in I_{LP1} when Q1 was turned off, which itself is a small fraction (typically less than one third) of the energy that was stored in this parasitic inductance when it was carrying the full load current, (I_L-I_M). As such, the energy lost in this second scenario is a very small fraction (typically less than one ninth) of the total energy originally stored in (or delivered to) L_{P1}, L_{P2}, C3 and C4. In other words, most of the parasitic energy is recovered.

Note that since the second scenario has a small amount of loss, it may be desirable to avoid this scenario by adjusting component values. One approach would be to make C3 and C4 bigger by augmenting the parasitic capacitors with explicit capacitors placed in parallel. With large enough values it is possible to ensure that the first scenario described above holds true for the full range of load currents expected.

The descriptions given above for both scenarios must be modified to account for the nonlinear nature of capacitors C3, C4, and C1, and also to account for the reverse recovery charge of the body diodes of Q3 and Q4. The details of the nonlinear waveforms are too complex to be described here, but the goal of recovering most of the parasitic energy is still achieved.

As mentioned previously, it is desirable to keep the overlap period as short as possible to minimize the time that the secondary currents are flowing through the body diodes of Q3 and Q4. It is also desirable to allow the energy recovering transitions just described to reach completion. These two competing desires can be traded off to determine an optimum overlap duration. In general, it is desirable to make sure the new primary switch is turned on before the old one is turned off, and that the portion of the half-cycle during which the uncontrolled rectifiers are conducting should, for efficiency sake, be less than 20%. Note that due to delays in the gate drive circuitry it is possible for the overlap interval to appear negative at some point in the control circuit.

The size of the output filter required to achieve a given output voltage ripple is affected by the AC ripple in the current of inductor L. This ripple current is largely caused by the switching action of the preregulation stage. A larger inductance, or a higher order filter for the output of the regulation stage, as shown in FIG. 6 where inductor L_B and capacitor C_B have been added, will reduce this ripple current.

The required size of the output filter is also affected by the AC ripple currents flowing in the magnetizing inductances of the transformers. Making these inductances as large as possible to reduce their ripple currents is therefore desirable. It is also beneficial to connect the tertiary reset windings back to a suitable point on the primary side as shown in FIG. 6A where they are connected to capacitor C_B, rather than to connect them to the output filter, as shown in FIG. 3. This alternative connection reduces by a factor of two the ripple current seen by the output filter due to the magnetizing inductance currents, compared to the connection shown in FIG. 3, since these magnetizing currents no longer flow to the output capacitor during their respective reset half cycles.

The power converter circuits described so far have all had an isolation stage that is current fed. It is also possible to incorporate the invention with an isolation stage that is voltage fed. By "voltage fed" it is meant that the voltage across the primary side of the isolation stage is held relatively constant over the time frame of the switching cycle. Such a converter circuit is shown in FIG. 6B where two uncoupled transformers are used.

The operation of the voltage-fed isolation stage is slightly different than for a current-fed isolation stage. Each primary transistor is still turned on for approximately one half the cycle, but instead of providing a brief overlap period during which both primary transistors, Q1 and Q2, are turned on together, here the primary transistors are both turned off for a brief overlap period.

During each half cycle, the current flowing into one primary winding and out its respective secondary winding can be determined as follows. Say transistors Q1 and Q3 have just been turned on to begin a new half cycle. At the completion of their switch transition they will be carrying some initial current (to be discussed in more detail below). There is also a difference between the voltage across capacitor C_B and the voltage across capacitor C_{OUT}, both reflected to the secondary side. This voltage differential will be called ΔV. It appears across the series circuit composed of the leakage/parasitic inductances and resistances of the primary and secondary windings, $T_{1,PRI}$ and $T_{1,SEC}$, the transistors Q1 and Q3, and the capacitors C_B and C_{OUT}. The current flowing through this series L-R circuit responds to the voltage across it, ΔV, in accordance with the component values, all referenced to the secondary side.

Since C_B and C_{OUT} are charged and discharged throughout the half cycle, ΔV will vary. But if we assume ΔV is relatively constant, then the current flowing through the series L-R circuit will change exponentially with an L/R

time constant. If this time constant is long compared to the duration of the half cycle, then the current will have a linearly ramping shape. If the time constant is short, that the current will quickly reach a steady value determined by the resistance.

To understand the switch transitions that occur between each half cycle, consider the leakage/parasitic inductances, L_{P1}, and L_{P2}, and the capacitances associated with the controlled rectifiers, C3 and C4, to be modeled in the same way as was shown in FIG. 5. Assume Q2 and Q4 have been on and are carrying a final current level, I_F, at the end of the half cycle. Transistor Q1 is then turned on, causing the voltage V_{CB} to be applied across primary winding T_{1PRI}, and its reflected value across secondary winding T_{1SEC}. An oscillation between C4 and L_{P1}, will ensue, with the voltage across C4 starting at approximately twice the output voltage. After approximately one quarter of a cycle of this oscillation, the voltage across C4 will attempt to go negative and be clamped by the body diode of Q3. At this point the current flowing through L_{P1}, will have reached a peak value, I_S, determined by approximately twice the output voltage divided by the characteristic impedance, $\sqrt{L_{P1}/C4}$. This transition discharges capacitor C4 and builds up the current in L_{P1}, to the value I_S in a nearly lossless manner.

During the quarter cycle of oscillation the voltage across the gate of transistor Q4 will drop below the threshold value for the device, and the channel of Q4 will turn off. The current that had been flowing through the channel will commutate to the body diode of Q4.

At this point current if flowing through both transformers' secondary windings and through the body diodes of Q3 and Q4. Q3 is carrying the current I_S and Q4 is carrying the current I_F. Now transistor Q2 is turned off and its voltage rises as parasitic capacitors are losslessly charged until the voltage is clamped by the diode in series with the tertiary windings, $T2_{TER}$. Inductor L_{P2} now has a negative voltage across it and its current I_{LP2}, will therefore linearly ramp down to zero as its energy is recovered back to CB through the clamping circuit. Once this current reaches zero, the body diode of Q4 will turn off and the current will become negative, but only to the point where it equals the second transform's magnetizing current, I_{MPK} (reflected to the secondary side). This current will linearly charge capacitor C3 nearly losslessly as energy is delivered to the capacitor from the magnetizing inductance of the second transformer (reflected to the secondary side). This current will linearly charge capacitor C3 nearly losslessly as energy is delivered to the capacitor from the magnetizing inductance of the second transformer.

As the voltage across C3 rises above the threshold value, transistor Q3 will turn on and the current that had been flowing through the body diode of Q3 will commutate to the channel of Q3. The new half cycle will then proceed as discussed above, with I_S being the initial value of current mentioned in that discussion.

As with the current-fed isolation stage, the transition between the two half cycles has a period of time when the two body diodes are conducting. This condition is highly dissipative and should be kept short by keeping the overlap period that both primary side transistors, Q1 and Q2, are off short.

In all of the power converter circuits described above, it might be desirable to slow down the switch transitions in the isolation stage for many reasons. For instance, slower transitions might reduce the high frequency differential-mode and common-mode ripple components in the output voltage waveform. There are several ways the switch transitions might be slowed down. For instance, in a well known manner a resistor could be placed in series with the gate of the primary side transistor Q1 (or Q2) in FIG. 5 so that its gate voltage would change more slowly. Similarly, a resistor could be placed in series with the gate of a synchronous rectifier Q3 or (Q4). In either case an RC circuit is created by the added resistor, R, and the capacitance, C, associated with the transistor. If this RC product is long compared to the normal length of the oscillatory transitions described above, the switch transitions will be slowed down.

If the length of the switch transitions are on the order of $\sqrt{(LC)}$ or longer, where L is the leakage/parasitic inductance (L_{P1} and/or L_{P2}) that oscillates with the capacitor C4 (or C3), then the nearly lossless transitions described above will not be achieved. The more the switch transitions are slowed down, the more the energy delivered to and/or recovered from the capacitors associated with the controlled rectifiers will be dissipated. As such, there is a tradeoff between the power converter's efficiency and its other attributes, such as output ripple content. This tradeoff might result in slower switch transitions in situations where high efficiency is not required or if better synchronous rectifiers in the future have much smaller capacitances.

As discussed above, the synchronous rectifier MOSFETs Q3 and Q4 in the circuit of FIG. 3 are driven with a gate-source voltage equal to approximately twice the output voltage. For a 5 volt output, the 10 volt drive that results is appropriate for common MOSFETs. If the output voltage is such that the gate drive voltage is too large for the ratings of the MOSFET, however, steps must be taken to reduce the drive voltage. For example, if the output voltage is 15 volts, a 30 volt gate drive will result, and it is typically desired that the gate be driven to only 10 volts. Also, some MOSFETs are designed to be driven with only 5 volts, or less, at their gates.

FIG. 7 shows one way to reduce the drive voltage while maintaining the energy recovery feature. The voltage waveform at node B (or at node A) is capacitively divided down by the series combination of capacitors Cs and C3 (or by C6 and C4). The values of these capacitors are chosen to provide the division of the AC voltage provided at node B (or node A) as desired. For example, if node B has a 30 volt step change and a 10 volt step change is desired at the gate of Q3, then C5 should have one half the capacitance of C3. Since C3 may be comprised of the parasitic capacitance of Q3, it is likely to be nonlinear. In this case, an effective value of capacitance that relates the large scale change in charge to the large scale change in voltage should be used in the calculation to determine C5.

Since a capacitor divider only divides the AC components of a waveform, additional components need to be added to determine the DC component of the voltage applied to the gates of Q3 and Q4. FIG. 7 shows one way to do this in which two resistors, R1 and R2 (or R3 and R4), provide the correct division of the DC component of the voltage at node B (or node A). These resistors should have values large enough to keep their dissipation reasonably small. On the other hand, the resistors should be small enough such that the time constant of the combined capacitor/resistor divider is short enough to respond to transients such as start-up.

Other techniques employing diodes or zener diodes that are known in the art could be used instead of the resistor technique shown in FIG. 7.

One variation of the invention described herein would be to create a power supply with multiple outputs by having more than one secondary winding on each transformer in the isolation stage. For example, by using two secondary wind-

ings with the same number of turns it would be possible to create a positive 12 volt output and a negative 12 volt output. If the two secondary windings have a different number of turns it would be possible to create two output voltages of different magnitudes (e.g., 5 volts and 3.3 volts). Another approach for creating multiple outputs would be to have multiple isolation stages, each with a turns-ratio appropriate for their respective output voltages.

When multiple outputs are provided in this manner, a phenomenon commonly called cross-regulation occurs. A single regulation stage cannot control the various output voltages independently, and these output voltages depend not just on the relative turns ratios, but also on the voltage drops that result as the various output currents flow through the impedances of their various output paths. A change in any one or more output currents therefore causes a change in the voltages of those outputs that are not used for feedback to the regulation stage. If this variation due to changes in output currents is a problem, then various approaches for providing regulation of the uncontrolled outputs can be provided. For example, a linear regulator might be added to each output that is not otherwise regulated.

One advantageous approach to providing linear regulation with the power circuits described here is to control how much the synchronous rectifier MOSFETs are turned on during their conduction state. This can be done by adding circuitry to limit the peak voltage to which their gates will be driven so that their on-state resistances can be made larger than their minimum values. It can also be done by controlling the portion of operative half cycle during which a MOSFET's gate voltage is allowed to be high so that the MOSFET's body diode conducts for the rest of the time. With both techniques, the amount to which the output voltage can be regulated is the difference between the voltage drop of the synchronous rectifiers when their channels are fully on (i.e., when they are at their minimum resistance) and when only their body diodes are carrying the current.

One way to accomplish the first technique, that of controlling the peak gate voltage, is to use the basic capacitor divider circuit that was shown in FIG. **7**. All that is needed is to make the resistor divider ratio, (or, alternatively, the diode clamping voltage if such an approach is chosen) dependent on a control signal derived from the error in the output voltage compared to its desired value. The goal is to shift the DC component of the gate voltage in response to the error signal such that the peak voltage applied to the gate, and therefore the on-state resistance and voltage of the synchronous rectifier, helps to minimize this error. Various control circuitry schemes that might be used to achieve this goal will be obvious to one skilled in the art. Note that this approach preserves the energy recovery feature of the gate drive. Note also that if the voltages at nodes A and B are such that no AC division is desired, then C**5** and C**6** should be made large compared to C**3** and C**4**.

FIG. **8** shows an alternative method to control the DC component of the gate voltage waveform. The output voltage (or a scaled version of it) is subtracted from a reference voltage and the error is multiplied by the gain of an op-amp circuit. The output of the op-amp (node C) is then connected to the synchronous rectifier gates through resistors that are large enough to not significantly alter the AC waveforms at the gates. With this connection, the DC components of the gate voltages will equal the output voltage of the op-amp at node C. If the gain of the op-amp circuit is large enough, such as when an integrator is used, the error in the output voltage will be driven toward zero. Z_F and Z_I, are impedances that should be chosen, with well established techniques, to ensure stability of this feedback loop while providing the gain desired.

The range of voltage required at the output of the op-amp depends on the particular application, and it may include negative values. This range influences the supply voltage requirements for the op-amp. Also, if the op-amp's output voltage gets too high, the synchronous rectifiers may not turn off when they are supposed to. Some means of limiting this voltage, such as a clamp circuit, may therefore be desirable.

One way to accomplish the second technique, that of controlling the portion of the half cycle in which the MOSFET is gated on, is to place a low power switch network between the gate of Q**3** (or Q**4**), node B (or node A), and ground. This network (composed, say, of analog switches operated with digital control signals) might be used to keep the gate voltage grounded for some period of time after the node voltage increases, and to then connect the gate to node B (or A) for the remainder of the half cycle with a switch capable of bidirectional current flow. The length of the delay would be based on a signal derived from the error in the output voltage. With this approach, the energy recovery feature associated with discharging each synchronous rectifier's gate capacitance is preserved, but the charging transition will become lossy. Alternatively, the switch network could be controlled to start out the half cycle with the gate connected to node B (or A), and then after some delay to connect the gate to ground.

Using a synchronous rectifier to provide regulation as well as rectification, as described above, is not limited to multiple-output situations. It can also be used in single-output situations either as the total regulation stage or as an additional regulation stage to augment the first one.

It is also possible to use DC-DC switching regulators on the secondary side to achieve the additional regulation desired, or to create more than one output voltage from any of the outputs of the isolation stage.

With multiple outputs it is not necessary for the gate of each controlled rectifier to be connected to secondary winding of the other transformer which corresponds to the same output. For instance, if the two outputs are 5 volts and 3.3 volts, the gates of the 3.3 volts output controlled rectifiers could be connected to the 5 volt output secondary windings. Doing so would give these controlled rectifiers a 10 volt gate drive, resulting in a lower on-state resistance than if they had a 6.6 volt gate drive.

In some situations, it may be desirable to place the isolation stage first in the power flow, and to have the regulation stage follow. For example, when there are many outputs sharing the total power, the circuit might be configured as one isolation/step-down (or step-up) stage followed by several DC-DC switching or linear regulators.

No matter where the isolation stage is situated, if it is to be current fed this requirement could be met with active circuitry as well as by a passive component such as an inductor. For instance, if the current fed isolation stage follows a regulation stage that is achieved with a linear regulator, then this linear regulator could be designed to have a large AC output impedance to achieve the input requirement of the current fed isolation stage.

When the regulation stage precedes the isolation stage, it is not necessary to sense the isolated output voltage to control the regulation. An alternative approach is to sense the voltage on the primary side of the isolation stage, which

may eliminate the need for secondary side circuitry and the need to bridge the feedback control signal across the isolation barrier.

For example, in FIG. **6** the voltage across C_B, the capacitor of the third-order output filter of the down converter, could be used. This voltage nearly represents the isolated output voltage (corrected for the turns-ratio). It differs only due to the resistive (and parasitic inductance commutation) drops between C_B and the output. Since these drops are small and proportional to the current flowing through the isolation stage, the error in output voltage they create can either be tolerated or corrected.

To correct the error, the current on the primary side could be sensed, multiplied by an appropriate gain, and the result used to modify the reference voltage to which the voltage across C_B is compared. Since these resistive drops vary with temperature, it might also be desirable to include temperature compensation in the control circuitry. Note that this approach could also be used to correct for resistive drops along the leads connecting the supply's output to its load.

The embodiments of the invention described above have used two uncoupled transformers for the isolation stage. It is also possible, as shown in FIG. **9**, to use a single transformer T in which, for example, there are two primary windings T_{PRI1}, T_{PRI2} and two secondary windings, T_{SEC1}, T_{SEC2}. While the two primary windings may be tightly coupled, either the two secondaries should be loosely coupled to each other or the connections to the output capacitors and synchronous rectifier transistors should provide adequate parasitic inductance. The resulting leakage and parasitic inductance on the secondary side can then be modeled as is shown in FIG. **9**.

With this inductance present in the secondary side loops, the operation of the coupled isolation stage during the overlap period is similar to what was described above for the uncoupled case. With Q**1** and Q**3** on, turn Q**2** on. The voltage across the transformer windings, as modeled in FIG. **9**, drops to zero, which is consistent with what must happen if the primary windings are tightly coupled. A nearly-lossless energy saving transition involving inductor/capacitor oscillations and linear discharges then ensues.

What is different here is that the overlap period during which both Q**1** and Q**2** are on cannot last too long. If the overlap lasts too long, the transient waveforms will settle into a state where the voltages at nodes A and B rise to the output voltage. If this voltage is higher than the gates' threshold levels, transistors Q**3** and Q**4** will partially turn on. A large amount of energy will then be dissipated while this state persists, and it is possible for the output capacitor to be significantly discharged.

These problems can be avoided by making sure the overlap period when both Q**1** and Q**2** are on does not last too long. For a given converter, an overlap period can be found which will give the highest converter efficiency. The more leakage/parasitic inductance there is, the longer an overlap period that can be tolerated. Based on the overlap time provided by a given control circuit, it may become necessary to add additional inductance by increasing the leakage or parasitic inductance.

With a coupled transformer it is not necessary to provide a separate reset circuit (whether it uses a tertiary winding or not) since the magnetizing current always has a path through which it can flow. With a coupled transformer it is necessary to keep the lengths of the two halves of the cycle well balanced to avoid imposing an average voltage across the core and driving it into saturation. Several techniques for balancing the two half cycles are well known in the art.

When two or more power supplies are connected in parallel, diodes are sometimes placed in series with each supply's output to avoid a situation where one supply's failure, seen as a short at its output, takes down the entire output bus. These "ORing" diodes typically dissipate a significant amount of energy. One way to reduce this dissipation is to replace the diode with a MOSFET having a lower on-state voltage. This "ORing" synchronous rectifier MOSFET can be placed in either output lead, with its body diode pointing in the direction of the output current flow.

With the invention described here, the voltage for driving the gate of this MOSFET, Q**5**, can be derived by connecting diodes to node A and/or node B (or to nodes of capacitor dividers connected to these nodes), as shown in FIG. **10**. These diodes rectify the switching waveforms at node A and/or node B to give a constant voltage suitable for turning on the ORing MOSFET at node D. A filter capacitor, C_F, might be added to the circuit as shown in the figure, or the parasitic input capacitance of the ORing MOSFET might be used alone. A resistor RF ensures the gate voltage discharges when the drive is removed.

If the power supply fails in a way that creates a short at its output, such as when a synchronous rectifier shorts, the voltages at nodes A and B will also be shorted after the transient is complete. With its gate drive no longer supplied, the ORing MOSFET will turn off, and the failed supply will be disconnected from the output bus.

When two (or more) power supplies of the type described here are placed in parallel, a problem can arise. If one power supply is turned on while another is left off (i.e. not switching), the output bus voltage generated by the first supply will appear at the gates of the second supply's synchronous rectifiers. Once this voltage rises above the threshold value, these synchronous rectifiers will turn on and draw current. At the least this will result in extra dissipation, but it could result in a shorted output bus. This problem can occur even if both supplies are turned on and off together if one supply's transition "gets ahead" of the other.

There are several approaches to solving this problem. One is to make sure both supplies have matched transitions. Another is to connect the supplies together with ORing diodes so that no supply can draw current from the combined output bus. If an ORing MOSFET is used instead of an ORing diode, however, this second approach can still fail to solve the problem. For instance, consider the case where a supply drives its ORing MOSFET with the technique shown in FIG. **10**. Assume the bus voltage is already high due to another supply, and the first supply is then turned on in a way that causes its output voltage to rise slowly toward its desired value. If the ORing MOSFET's gate voltage rises high enough to turn it on before the newly rising output voltage approximately matches the existing bus voltage, then there will be at least a momentary large current flow as the two voltages equalize. To avoid this problem additional circuitry can be added to make sure an ORing MOSFET is not turned on until its supply's output voltage has approximately reached the bus voltage. This might be done by sensing the two voltages and taking appropriate action, or it might be done by providing a delay between when the ORing MOSFET's gate drive is made available and when it is actually applied to the gate. Such a delay should only affect the turn-on, however; the turn-off of the ORing MOSFET should have minimal delay so that the protective function of the transistor can be provided.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various

changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. Those skilled in the art will recognize or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments of the invention described specifically herein. Such equivalents are intended to be encompassed in the scope of the claims. For instance, the regulation stage could be composed of an up-converter. The ideas that have been presented in terms of the N-channel implementation of the synchronous rectifier MOSFET can be modified to apply to the P-channel implementation, as well. The components shown in the schematics of the figures (such as Q3 in FIG. 3) could be implemented with several discrete parts connected in parallel. In addition, certain aspects of the invention could be applied to a power converter having only one primary transformer winding and/or one secondary transformer winding.

What is claimed is:

1. A power converter system comprising:

a DC power source;

a non-regulating isolation stage comprising:

a primary transformer winding circuit having at least one primary winding connected to the source; and

a secondary transformer winding circuit having at least one secondary winding coupled to the at least one primary winding and having plural controlled rectifiers, each having a parallel uncontrolled rectifier and each connected to a secondary winding, each controlled rectifier being turned on and off in synchronization with the voltage waveform across a primary winding to provide an output, each primary winding having a voltage waveform with a fixed duty cycle and transition times which are short relative to the on-state and off-state times of the controlled rectifiers; and

a plurality of non-isolating regulation stages, each receiving the output of the isolation stage and regulating a regulation stage output while the fixed duty cycle of the isolation stage is maintained.

2. A power converter system as claimed in claim 1 wherein the regulation stages are switching regulators.

3. A power converter system as claimed in claim 2 wherein the regulation stages are down converters.

4. A power converter system as claimed in claim 2 wherein a switch in the switching regulator is a controlled rectifier.

5. A power converter system as claimed in claim 1 wherein the first and second controlled rectifiers are voltage controlled field effect transistors.

6. A power converter system as claimed in claim 1 wherein the DC power source has a voltage-fed output characteristic.

7. A power converter system as claimed in claim 2 wherein the voltage fed output characteristic of the DC power source is provided by a capacitor.

8. A power converter system as claimed in claim 1 wherein the signal controlling a controlled rectifier is provided by a transformer winding.

9. A power converter system as claimed in claim 1 wherein the output of the isolation stage is about 12 volts.

10. A power converter system as claimed in claim 9 wherein the regulation stage output is of a voltage level to drive logic circuitry.

11. A power converter system as claimed in claim 1 wherein energy is nearly losslessly delivered to and recovered from capacitors associated with the controlled rectifiers.

12. A power converter system as claimed in claim 1 wherein each controlled rectifier is turned on and off by a signal applied to a control terminal relative to a reference terminal of the controlled rectifier and the reference terminals of the controlled rectifiers are connected to a common node.

13. A power converter system as claimed in claim 1 wherein the isolation stage is a step down stage.

14. A power converter system as claimed in claim 1 wherein the regulation stage output is of a voltage level to drive logic circuitry.

15. A power converter system as claimed in claim 14 wherein the regulation stage output is about 5 volts or less.

16. A power converter system as claimed in claim 14 wherein the regulation stage output is about 3.3 volts.

17. A power converter system as claimed in claim 1 wherein the DC power source provides a voltage that varies over the range of 36 to 75 volts.

18. A power converter system as claimed in claim 1 wherein the DC power source provides a voltage within the range of 36 to 75 volts.

19. A power converter system as claimed in claim 18 wherein the regulation stage output is of a voltage level to drive logic circuitry.

20. A power converter system comprising:

a DC power source;

a non-regulating isolation stage comprising:

a primary transformer winding circuit having at least one primary winding connected to the source; and

a secondary transformer winding circuit having at least one secondary winding coupled to the at least one primary winding and having plural controlled rectifiers, each having a parallel uncontrolled rectifier and each connected to a secondary winding, each controlled rectifier being turned on and off in synchronization with the voltage waveform across a primary winding to provide an output; and

a plurality of non-isolating regulation stages, each receiving the output of the isolation stage and regulating a regulation stage output.

21. A power converter system as claimed in claim 20 wherein the regulation stages are down converters.

22. A power converter system as claimed in claim 20 wherein the signal controlling a controlled rectifier is provided by a transformer winding.

23. A power converter system as claimed in claim 20 wherein the isolation stage is a step down stage.

24. A power converter system as claimed in claim 20 wherein the DC power source provides a voltage within the range of 36 to 75 volts.

25. A power converter system as claimed in claim 20 wherein the output of the isolation stage is about 12 volts.

26. A power converter system as claimed in claim 25 wherein a regulation stage output is of a voltage level to drive logic circuitry.

27. A power converter system comprising:

a DC power source;

an isolation stage comprising:

a primary transformer winding circuit having at least one primary winding connected to the source; and

a secondary transformer winding circuit having at least one secondary winding coupled to the at least one primary winding; and plural controlled rectifiers,

each having a parallel uncontrolled rectifier and each connected to a secondary winding, each controlled rectifier being turned on and off in synchronization with the voltage waveform across a primary winding to provide an output voltage whose value drops with increasing current flow through the isolation stage; and

a plurality of non-isolating regulation stages, each receiving the output of the isolation stage and regulating a regulation stage output.

28. A power converter system as claimed in claim **27** wherein each primary winding has a voltage waveform with a fixed duty cycle and transition times which are short relative to the on-state and off-state times of the controlled rectifiers.

29. A power converter system as claimed in claim **27** wherein the isolation stage is non-regulating.

30. A method of providing multiple DC outputs comprising:

from a DC power source providing an isolated output without regulation by applying power through at least one primary winding connected to the source and at least one secondary winding coupled to the at least one primary winding, the at least one secondary winding being in a secondary transformer winding circuit having plural controlled rectifiers, each having a parallel uncontrolled rectifier and each connected to a secondary winding, each controlled rectifier being turned on and off in synchronization with the voltage waveform across a primary winding to provide an isolated output; and

from the isolated output, providing plural regulated outputs without further isolation.

31. A method as claimed in claim **30** wherein each primary winding has a voltage waveform with a fixed duty cycle and transition times which are short relative to the on-state and off-state times of the controlled rectifiers.

32. A method as claimed in claim **30** wherein the isolated output is a voltage whose value drops with increasing current flow.

33. A method of providing multiple DC outputs comprising:

from a DC power source providing an isolated output by applying power through at least one primary winding connected to the source and at least one secondary winding coupled to the at least one primary winding, the at least one secondary winding being in a secondary transformer winding circuit having plural controlled rectifiers, each having a parallel uncontrolled rectifier and each connected to a secondary winding, each controlled rectifier being turned on and off in synchronization with the voltage waveform across a primary winding to provide an isolated output, the isolated output being a voltage whose value drops with increasing current flow; and

from the isolated output, providing plural regulated outputs without further isolation.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

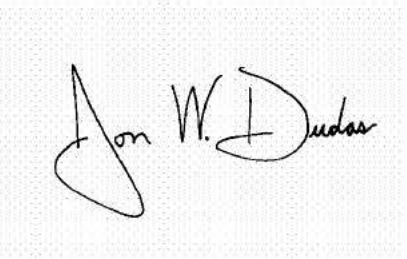
PATENT NO. : 7,072,190 B2
APPLICATION NO. : 10/812314
DATED : July 4, 2006
INVENTOR(S) : Martin F. Schlecht

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 17
Claim 7, line 57, delete "2" and insert --6--.

Signed and Sealed this

Twenty-first Day of November, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

CERTIFICATE OF FILING AND SERVICE

I hereby certify that on September 2, 2014, I electronically filed the foregoing with the Clerk of Court using the CM/ECF System, which will send notice of such filing to the following registered CM/ECF users:

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I further certify that, upon acceptance and request from the Court, the required paper copies of the foregoing will be deposited with United Parcel Service for delivery to the Clerk, UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT, 717 Madison Place, N.W., Washington, D.C. 20439.

The necessary filing and service were performed in accordance with the instructions given to me by counsel in this case.

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CERTIFICATE OF COMPLIANCE
With Type-Volume Limitation, Typeface Requirements, And Type Style Requirements

1. This brief complies with the type-volume limitation of Fed. R. App. P. 32(a)(7)(B) because:

   this brief contains 13,596 words, excluding the parts of the brief exempted by Fed. R. App. P. 32(a)(7)(B)(iii).

2. This brief complies with the typeface requirements of Fed. R. App. P. 32(a)(5) and the type style requirements of Fed. R. App. P. 32(a)(6) because:

   this brief has been prepared in a proportionally spaced typeface using Microsoft Word 2013 in 14pt Century Schoolbook

Dated: September 2, 2014

/s/ Matthew A. Smith
Matthew A. Smith